Computer Controlled MHD Power
Consolidation and Pulse Generation System

Final Technical Progress Report
Oct. 1987 - Aug. 1990

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Electronics Research Laboratory

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GLOSSARY OF TERMS

Term or Abreviation	Description
ac	alternating current
A/D	Analog-to-Digital
ASIC bus	Application specific integrated circuit bus
CFT	continuous Fourier Transform
consolidation	the consolidation of multiple-dc sources into a single source
dc	direct current
diagonal mode	MHD connection employing both Hall and Faraday fields
EMTP	Electro-Magnetics-Transient-Program (EPRI)
EPRI	Electric Power Research Institute, Palo Alto, CA
Faraday mode	MHD connection employing only the Faraday electric field
GTO	Gate-Turn-Off thyristor switch
Hz	Hertz, frequency in cycles/second
inversion	The process of generating ac waveforms from dc sources
I/O	Input-output
MHD	Magnetohydrodynamic
Mosfet	Metal oxide semiconductor field effect transistor
Mux	Multiplexor, many-to-one consolidation
MWe	Megawatts electric
PASC	Pulse-Amplitude-Synthesis-and-Control
RTX	Real-Time-Express (Harris Corporation trademark)
RTXEB	RTX evaluation board
SBC	single board computer
snubber	a sub-circuit to allow for continuity of current flow through a switched inductor
SPICE	Simulation Program for Integrated Circuit Evaluation
SRAM	static random access memory
Tesla	Measure of magnetic flux density = 10^4 Maxwells
Thevenin equivalent	Network theorem equivalent terminal voltage and impedance representation
thyristor	non-reciprocal threshhold voltage circuit element
Tri-state	solid state device providing latching of temporary bus information signals
UART	Universal Asynchronous Receive and Transmit circuit

2.0 INTRODUCTION

The major goal of this research project is to establish the feasibility of a power conversion technology which will permit the direct synthesis of computer programmable pulse power. Feasibility has been established in this project by demonstration of direct synthesis of commercial frequency power by means of computer control. The power input to the conversion system is assumed to be a Faraday connected MHD generator which may be viewed as a multi-terminal dc source and is simulated for the purposes of this demonstration by a set of dc power supplies. This consolidation/inversion (CI), process will be referred to subsequently as Pulse Amplitude Synthesis and Control (PASC).

A secondary goal is to deliver a controller subsystem consisting of a computer, software, and computer interface board which can serve as one of the building blocks for a possible phase II prototype system.

3.0 WORK PROGRESS

This report period work summarizes the accomplishments and covers the high points of the two year project. Progress is reported by reference to the original contract, and includes discussions on the following areas:

Comparison of the original PASC concept as proposed at the project inception, the Feasibility Demonstration system design, and the final resulting concept at the end of the project.

Preliminary computer simulation results from applying the PASC technology to the diagonal generator connection.

Feasibility Demonstration Test results using low-level power semiconductors.

Feasibility Demonstration Test results obtained using intermediate-level power semiconductors.

Description of some preliminary harmonic suppresion control waveform algorithms and a new data acquisition system and control system.

Final calculation results for a space-deployed minimum power-to-weight ratio PASC system at a 100 MWe level.

3.1 PASC Concept Evolution and Comparisons: Inception, Feasibility Demonstration, Inductive and Capacitive Consolidation, and Single Terminal.

The original PASC concept at contract inception is shown in Figure 1 in block diagram form for a Faraday connected MHD generator.
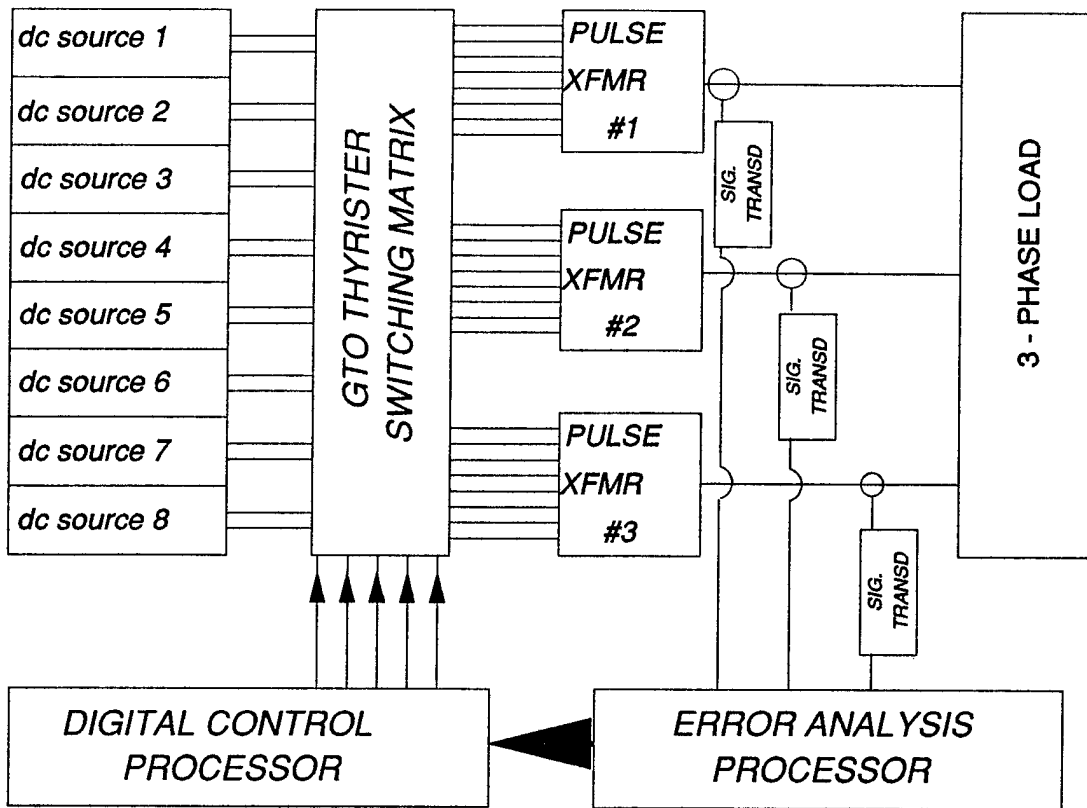
Figure 1. PASC Faraday-connected Consolidation/Inversion System For 8 Sources

A quite complex transformer was originally envisioned assuming that only a single transformer was going to be used for consolidating all of the Faraday individual dc sources along with generation of a single phase alternating current waveform. Although consolidation and superposition using the PASC concept can be implemented either magnetically using inductors or capacitively with capacitors, inductors were chosen for the Feasibiltiy Demonstration design because they are generally lower in cost, more rugged, and provide significant voltage isolation between windings. Negative aspects of transformers include their weight, nonlinearities, requirement that no average dc signals be present, and somewhat higher losses compared to capacitors per unit of energy storage. At the beginning it was not realized how important exact magnetic symmetry was for proper balancing of power output over the transformer(s) as is indicated in Figure 2 which shows asymmetry of magnetic circuit coupling depending on the location of the primary windings. Subsequent experimental results along with computer analysis show that symmetry of coupling coefficients, losses, etc., are quite important for achieving minimal loss performance, symmetry with respect to saturation effects, and wide frequency bandwidth of operation which are neccesary for pulse applications. Other changes from the original inception diagram shown in Figure 2 included:
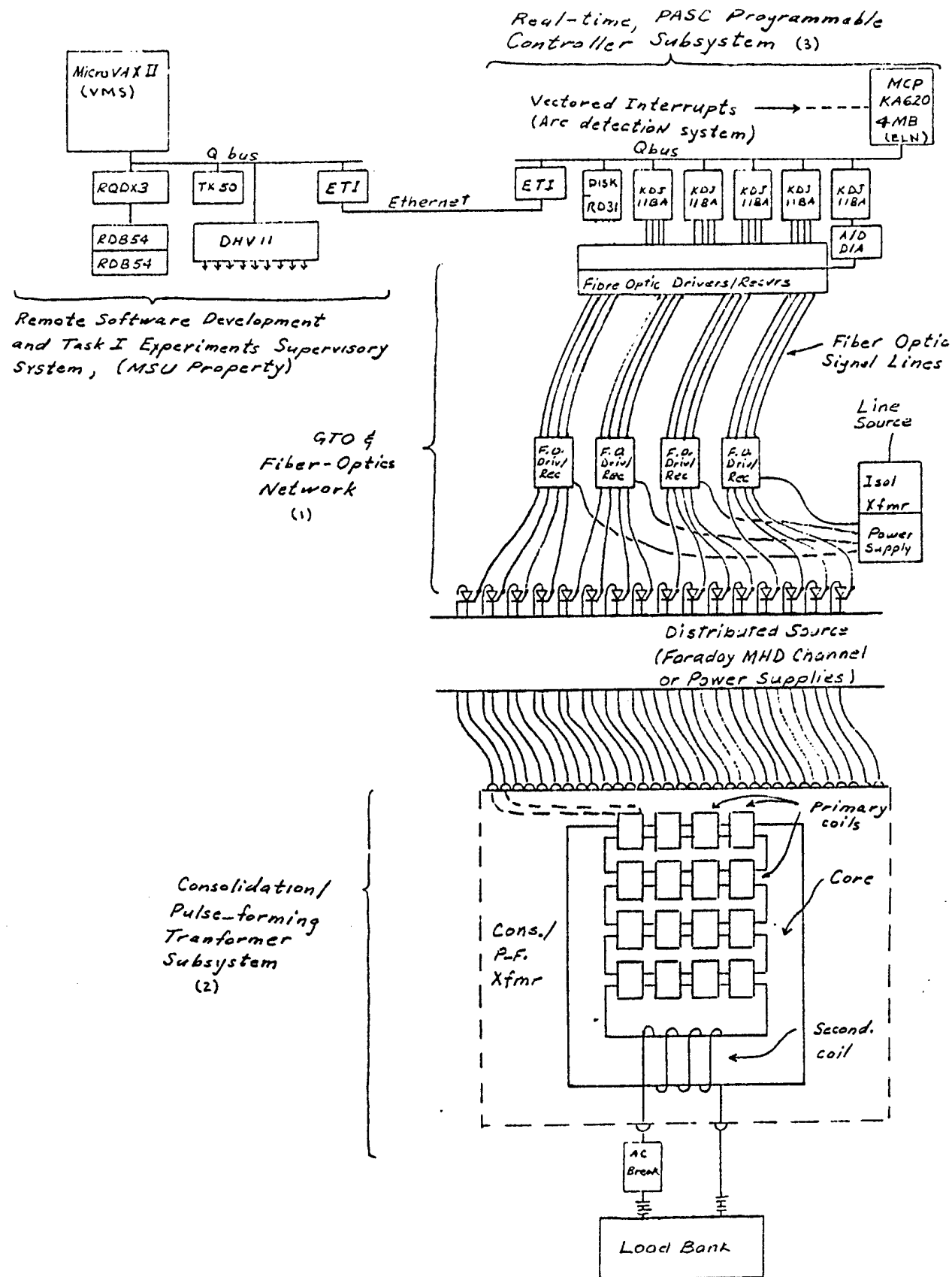
Figure 2 Early Conceptual PASC System Diagram

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a. The usage of optically isolated computer level switching transistors rather than fiber optics circuits to achieve isolation of the computer control circuitry from the heavy current test circuity. In an actual system fiber optics would be used because the power voltages would exceed tens of kilovolts whereas in the Feasibility Demonstration system all voltages were less than one kilovolt. Such an isolation system is indicated in Figure 3.
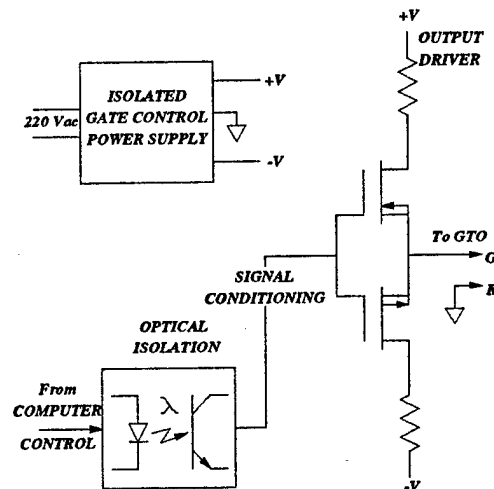
Figure 3. Optical Isolation Computer-to-Switching Interface

b. Because of cost and time considerations it was decided at the time of detailed design of the Feasibility Demonstration system to only implement a single-phase rather than a three-phase inverter system. A three phase inverter system involves no additional design or demonstration unknowns relative to a single-phase system: it consists of three, single-phase inverters connected in parallel across the sources as shown in Figure 4.
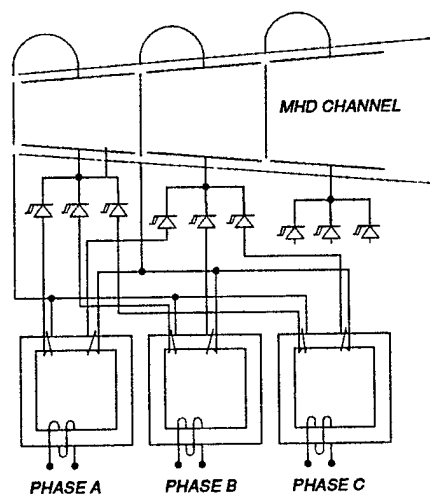
Figure 4. Adjacent Electrode Parallel Loading to Obtain Bipolar consolidation and three-phase Inversion

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c. Rather than use a remote Microvax II processor to develop the software for PASC GTO switching control with network down-line loading to a dedicated control Microvax II running the ELAN real-time operating system, the control Microvax II was purchased with the VMS operating system. Software was then developed directly on the Microvax II and down-loaded into a slave KXT-11 processor using a software loader purchased form Digital Equipment Corporation. This permitted the Microvax II to be the master control computer with the KXT-11 processor being the dedicated slave processor for control of the PASC switching signals. The Microvax II was also used to collect and store the experimental data from the PASC Feasibility Demonstartion system. For a three phase power system it would require one KXT-11 slave processor per phase if a eight-pulse height system is to be constructed. The required control configuration for single phase is shown in Figure 5.
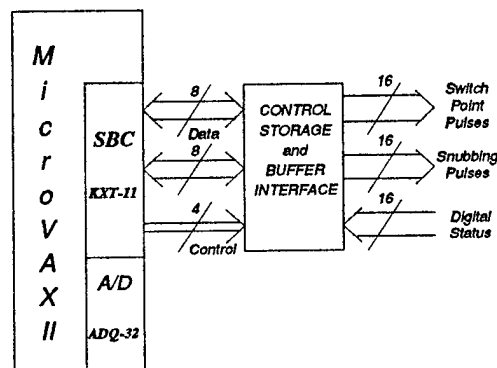
Figure 5. DEC Microvax II Master Controller with KXT-11 SBC Slave Switching Control Sequencer

Also shown in Figures 3 and 5, is the KXT-11 Interface and Gate firing circuit. Interfacing with the 20-line parallel I/O port signals generated by a Z-CIO (Z8536 Counter/timer and Parallel I/O), chip on the KXT-11 board and the PASC switching circuitry is provided using standatd TTL LS series logic units. The 8-bit A and B port signals are stored in two 16-bit registers made up of tri-state octal D-type transparent latch units (74LS373), under controls generated by the 4-bit C-port signals. The 32 outputs of these registers (SA0-SA15,SB0-Sb15), contain the control information for each Gate-Turn-Off (GTO), thyristors in the PASC switching system.

Each GTO switch point is controlled by a Gate-Firing-Circuit (GFC). The 32 outputs from the 16-bit registers drive the optical isolator units of the GTO GFC's. These optical units provide the isolation required between the control signals of the various GTO switch points. The isolator output drives a buffering stage which in turn drives the complementary symmetry MOSFET driver of the GTO gate-cathode circuit. The MOSFET driver provides low-impedance turn-on (.3 amperes), and turn-off (1 ampere), sources required for the high speed switching of the low power GTO units. GFC power is supplied by isolated auxiliary plus or minus 9 vdc supplies. A resistor change on the GFC board allows approximately 1 ampere of turn-on driver required for the high power GTO units.

After the need for symmetry became known (both through experimental data and computer simulation), an intermediate design which produced high symmetry was hand constructed as shown in Figure 6.

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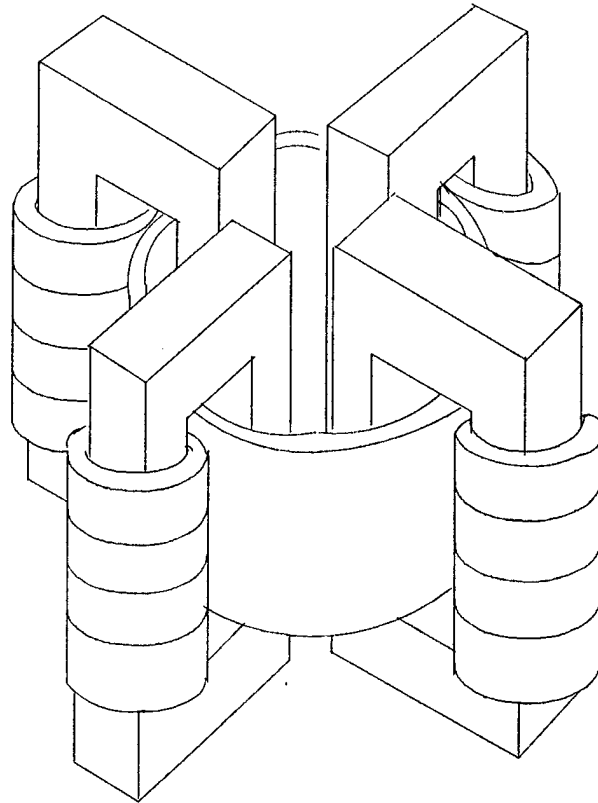
Figure 6. Four Core, 16 Primary, Parallel Secondary PASC Transformer

The original design contained four primary windings per outside transformer web, with a total of 16 primary windings on four webs. This transformer is referred to as a four-core, 16 primary, parallel secondary PASC transformer configuration. All transformers were identically coupled to a single secondary winding occupying the common central web of the transformer. Because of the voltage "leakage" effect (flux is instantaneously conserved, not voltage), when more than a single primary is active on a superpositon transformer, this transformer produced a very poor (non-sinusoidal), output when all of the primary windings are energized. However, when operated with single active primary per superposition web, the transformer gave excellent results. An additional, optional, central square piece of transformer iron can be added to this design in order to increase the coupling and mutual inductance if desired but further testing of this configuration is necessary in order to validate that this will not result in "voltage leakage" for some input pulse sequences.

Because of a desire to go to a full 16 pulse superposition, and a desire to minimize transformer design and fabrication costs for this research, the multiple web single transformer was set aside in favor of multiple, magnetically isolated but with series, current coupled secondaries. This greatly simplified the computer simulation of the device using either SPICE or our dedicated Fortran programs as well as facilitating the possible use of standard, off-the-shelf distribution transformers for the PASC demonstration design.

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The final configuration chosen for the PASC Feasibility Demonstration design consisted of eight transformers each of which contained two primaries and a single secondary winding. This produced a design in which one primary winding on each transformer was used for generation of positive-going pulses and one primary was used for negative-going pulses, thus achieving the desired result of having only one primary active per transformer so as to avoid the voltage "leakage" effect mentioned previously. To achieve superposition of the pulse outputs, all of the secondaries of the eight transformers were connected in series as shown in Figure 7.
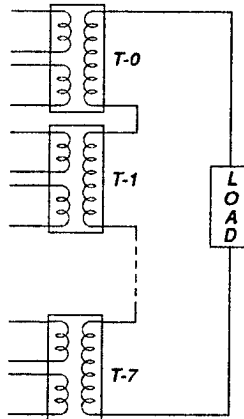
Figure 7. Two-Primary Winding CI Transformers With Series Connected Secondaries.

To achieve no voltage leakage occurance for those time intervals when only certain of the transformers are active, all primaries of non-active transformers were kept shorted. This guaranteed that the voltage drop across all of the non-active transformer secondaries would be minimal. To test the thesis that voltage leakage could be avoided by shorting of the primaries of all non-active transformers a set of generic transformers which were left over from another research project were used. These transformers produced very satisfactory results but were not useful for the Feasibility Demonstration tests because they lacked two primary and two secondary windings so that both step-up and step-down configurations could be tested. They also had a non-ideal turns ratios and values for self inductances. Results for step-down testing of these transformers were so satisfactory that it was decided to do the Feasibility Demonstration testing using small standard power distribution transformers similar to the generic transformers but with two primary and two secondary windings and greater primary and secondary inductances. General Electric transformers satisfying these requirements were then ordered and refitted into the PASC demonstration system.

3.2 Preliminary computer simulation results from applying the PASC technology to the diagonal generator connection.

Although not called for in the work statements, the application of PASC technology to diagonally connected MHD generators is of considerable interest for commercial applications if very low harmonic content power frequency waveforms can be easily generated on diagonal configuration MHD generators. One implementation of the PASC concept to MHD diagonally connected generators can be achieved by means of parallel excitation of a group of primary transformer windings whose secondaries are then connected in series as shown in Figure 8. This configuration is a straightforward extension of the PASC technology

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already demonstrated for Faraday type connection: the primaries of all of the transformers are connected in parallel across the two-terminal output of the MHD generator rather than individual electrode pairs.

Bipolar Pulse MHD Diagonal Consolidation/Inversion
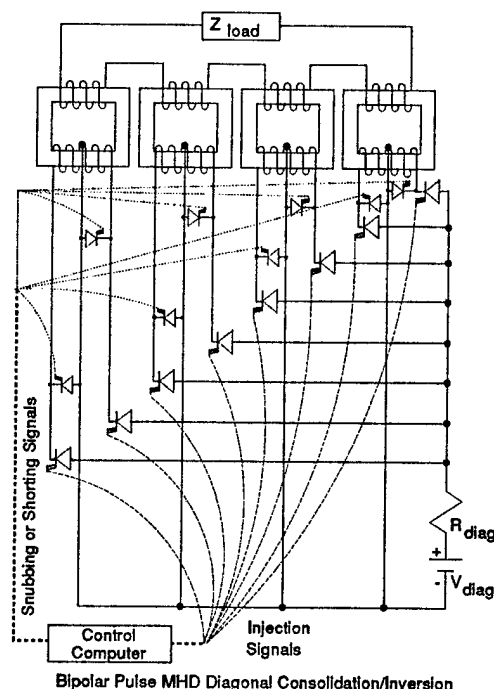
Figure 8.   PASC Four-pulse CI System For A Diagonally Connected MHD Generator

Shown in Figure 8 is the circuitry for a single phase inverter waveform synthesis consisting of four positive and four negative pulses which are produced by time multiplexed switching of the eight GTO power injection thyristors indicated. A more typical commercial system would consist of eight transformers in order to achieve desired low harmonic content without filtering. A standard three-phase inverter would be constructed by placing three such circuits in parallel across the diagonal voltage source V_{diag}. The three single-phase inverters would then be synchronized with the same control computer so as to produce the usual phase shifted three-phase output. All of the required computer switching and control interface technology is identical to that already developed for the SDI PASC Feasibility Demonstration Project; only the software control algorithm must be changed for this diagonal connected PASC application. The synthesis mode indicated in Figure 7 is only one method of carrying out the necessary waveform synthesis; other methods using proprietary circuitry are being investigated.

Results are discussed below for simulations involving a Thevenin equivalent circuit to represent the MHD generator, in which the resistor shown in Figure 8 represents the local ratio of diagonal open-circuit voltage to short-circuit diagonal current. Since no measurable values are directly available for this data (they might be extrapolated from data for some existing generators), per unit dimensionless values in the range of 1 to 100 ohms have been assumed, (see Rosa[1] Fig. 4.6, p. 66). The results shown were obtained using the Electromagnetic Transients Program (EMTP), to integrate the circuit configuration given.

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The results indicate that a sinusoidal load voltage and current can be obtained if the internal Thevenin series resistance is small in comparison with the load voltage. Even if the internal impedance is higher, sinusoidal output can be guaranteed by placing a smoothing electrolytic capacitor across the diagonal terminals. Although no closed loop harmonic suppression control is applied, the resulting waveforms have very low harmonic content, particularly for the case in which the load impedance is 100 ohms and the internal generator impedance is 1 ohm.

3.2.1 Modeling the PASC Process Using EMTP

The EMTP[2] program is a standard in the utility industry which is used to study switching transients on power distribution networks and high-voltage transmission lines. It has detailed models for actual power transformers but does not represent power semiconductors well (especially GTOs); these are modeled in the present simulations as ideal switches which is close to reality as far as the load voltage-current results are concerned while of course not providing any detail as to GTO internal behavior. SPICE[3] could also be used to model the PASC process but it has very poor transformer models. EMTP's advantage for this study is that it is possible to model the PASC network at the systems level very rapidly without a lot of programming. Because EMTP is usually applied to very large networks with requirements for integrating very large state vectors, it utilizes trapezoidal integration to cut integration time and is absolutely stable but also is known to be inaccurate in local behavior. Thus, based upon other simulations we know that the results presented herein are correct in general behavior but the instantaneous behavior immediately after switching points is somewhat in error because the trapezoidal integration does not handle optimally the opening of switches on inductors. We can compensate for this by placing high values of resistance across the switching contacts (that is by introducing dissipation), but the values are then somewhat attenuated with respect to the correct solution. Thus in the results which follow the sharp spikes or local oscillations in the waveforms are incorrect; both Runge-Kutta and Adams-Bashforth integrations of a very few simulations have verified this), but the gross or average value of the waveforms is quite close to the correct values.

As can be observed in all of the results, the sharp sawtooths in the waveform only occur at the switch opening points on the inductors. This behaviour is major reason that a more robust integration algorithm is planned for the next release of EMTP.

3.2.2 Discussion of Results:

The results show the strong effect of (source impedance)/(load impedance) ratio on the resulting waveform. All results shown are for a transformer step up ratio of 1:2 and are the result of superimposing the outputs in series of eight transformers secondaries. No attempt has been made to perform any control on the superposition widths of the pulses making up the waveform other than the standard sinusoidal modulation which has been used for the Faraday PASC configuration of eight similar transformers. Thus considerable additional harmonic suppression capability is possible beyond the present results. The only waveform that is really acceptable is for the case of $R_{source} = 1\Omega, R_{load} = 100\Omega$. As previously stated, no attempt has been made so far to model the MHD generator in a more realistic manner.

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Figure 9 show the output current for a Thevenin source resistance of 10 ohms, and a load resistance of one ohm. The primary source impedance relects into the secondary by the step-up turns ratio squared, or 40 ohms. Thus for the series secondary connection, as the number of active transformer secondaries increases with time during the sinusoidal synthesis process, they couple to the secondary side of the transformers greater and greater amounts or reflected primary source impedance until this reflected impedance dominates the the secondary load impedance. This coupled or time dependent secondary impedance depends only on the source impedance and the turns ratio of the transformers. During the rise from one active transformer to eight transformers, the reflected secondary transformer impedance increases from 40 to 320 ohms. Hence, for the source impedance of ten ohms, all loads except for very large load impedances, (and hence very low loading) the response shown in Figure 9 is to be expected and will be unsatisfactory for commercial application.

Figures 10, 11, and 12 are for a source impedance of 1 ohm which reflects into the secondary as 4 ohms for a single transformer to 32 ohms as all eight transformers become active. Thus for the case shown in Figure 10, with a load impedance of 100 ohms, the load impedance at a minimum is still more than three times the maximum reflected source impedance and the resulting load current is nearly sinusoidal in form. In the cases indicated in Figures 11 and 12, the load impedance becomes less than 1/3 and less than 1/30 respectively of the maximum reflected source impedance with again, highly non-sinusoidal output.

In summary, what does this say about power from a diagonally connected MHD generator? The source impedance of a MHD generator is quite low, varying typically from .005 ohms to .2 ohms for liquid metal to gaseous coal fired MHD generators. Hence if the diagonal voltage is not too low, a relatively moderate voltage step up will be required to meet utility conditions and thus there should not be any trouble guaranteeing very low harmonic content for this C/I technology. As a matter of perspective, the internal impedance of most large commercial ac generators is of the order of one ohm so that they should be at least as poor as MHD in this regard. However, they now typically generate directly up to 26,000 terminal volts which is somewhat beyond most present MHD designs.

Figure 9

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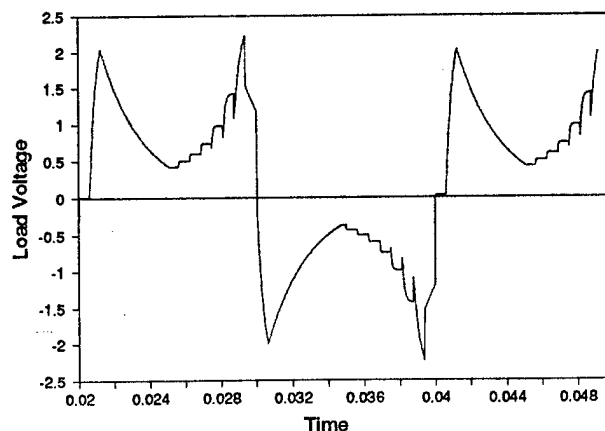
Diagonal Config. Rsource=1, Rload=100
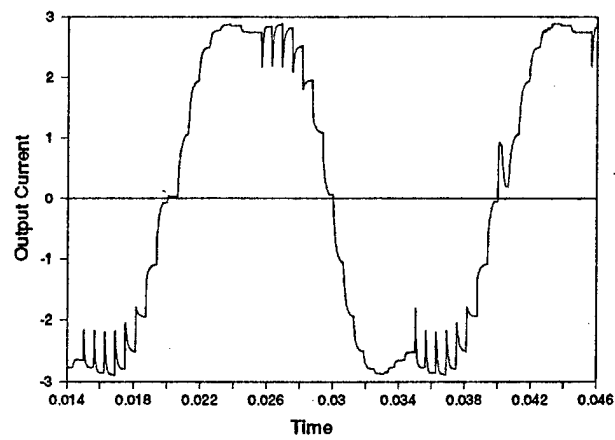
Figure 10

Diagonal Config. Rsource=1, Rload=10
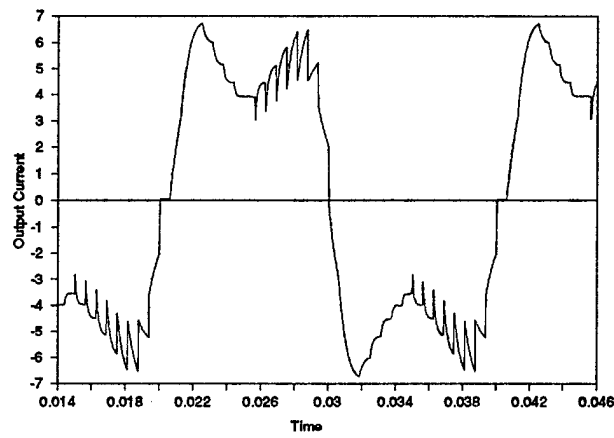
Figure 11

Diagonal Config. Rsource=1, Rload=1

Figure 12

17
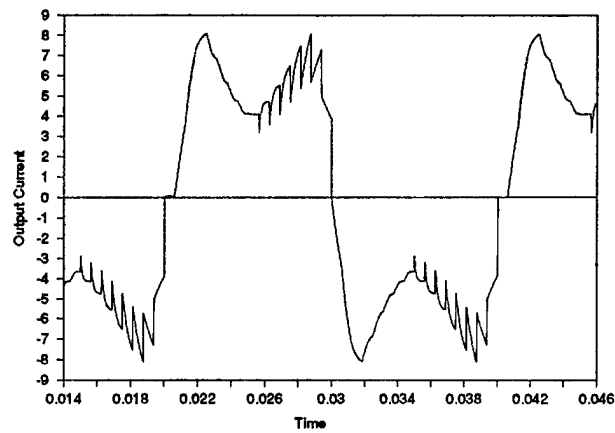
3.3 Feasibility Demonstration Test Results Using Low Power Semiconductors

The Feasibility Demonstration Test of the PASC technology was conducted on Wednesday, August 16, 1989 in the Electrical Engineering Laboratories at Montana State University with representatives from the PETC DOE/MHD office, W.J. Schaffer Associates, support contractor for DOD MHD/SDIO, Mountain States Energy, and DOE/INEL. Although the results were reported previously, the Feasibility Demonstration Test Agenda and Results were performed with low-power GTO semiconductor switches. The agenda and results of the low power tests are summaraized here for completeness and for comparison with the intermediate-power test results given in section 3.4. Detail result figures for the low power semiconductor tests were given in previous reports.

The scheduled agenda included:

a. A presentation on the theory and design of the PASC hardware system, the computer control and programming system, the computer switching - GTO interface, The source d.c. power supply design, the GTO switching power supply design, preliminary simulation results of several input waveforms, and results obtained previously using generic transformers in parallel and series connections.

b. A laboratory demonstration of the PASC system operating with the new transformers connected in series secondary connection, step-down voltage configuration. Responses using both high and low impedance snubbing, variable programmed output waveform and frequency, and variable output load impedance were demonstrated.

c. Following a break to permit re-connection of the transformers in step-up configuration, the laboratory demonstrations were repeated. Finally, several pulse waveforms not called for in the work statements were demonstrated.

d. Following the demonstration, a session devoted to requirements for possible application to various weapon systems was held. These included generic FEL and NPB type devices.

e. Finally, an exit session was held in which PETC DOE/MHD contract technical management indicated that an estimate of the power/weight ratio for a PASC power conversion system at the 100 MEW level would be useful.

The waveforms demonstrated in detail included algorithms approved as part of the Feasibility Demonstration Test Plan. Programming of the KXT-11 slave GTO control processor was demonstrated by performing several test algorithms called for in the statement of work.

These algorithms included:

b.1 A 60 Hz symmetric sawtooth waveform constructed from the superposition of eight positive pulses and eight negative pulses. Since the required delay between pulses to produce this waveform is uniform, it will sometimes be referred to subsequently as a constant delay triangular waveform.

b.2 A 60 Hz sinusoidal approximation waveform constructed from eight positive and eight negative pulses which are switched at time delays to give a best fit to the sinusoidal waveform if the system is behaving linearly.

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b.3   A zero delay symmetric waveform constructed from eight positive and eight negative pulses which are gated on sequentially at the maximum rate that the KXT-11 can perform. Since the delays are all the same number of KXT-11 machine cycles, the resulting waveform turns out to be a sawtooth waveform at approximately 600 Hz.

b.4   A very slow cycling of the GTO switching cycle sequence, not intended for powered operation, but for checking the proper sequencing of main and snubbing GTO switching signals by means of a light emitting diode array.

b.5   In addition to the above waveforms, both a bipolarity rectangular pulse waveform and a bipolarity ramp waveform were generated.

Loads for which successful waveform synthesis operation was demonstrated included: open circuit, 100 ohms, and 10 ohms. Linearity of response was demonstrated at all load conditions in step-down connection configuration while step-up configuration demonstrated linear response to open circuit and 100 ohm loading with non-linear compression at the 10 ohm loading. The compression in at the 10 ohm loading is caused by the very low impedance reflected into the d.c. source side of the PASC transformer with a resulting large voltage drop occurring across the Thevenin source impedance rather than the PASC transformers.

3.3.1   Summary of PASC Feasibility Demonstration Low-power Test Results

3.3.1.1   The master/slave computer control switching system performs as designed and programmed. The KXT-11 slave switching processor can successfully generate sinusoidal algorithm commutation pulses with variable delay requirements up to approximately 300 Hz for 16 primary GTO switches and 16 snubbing GTO switches. With no time delays (linear triangular pulses), the maximum frequency that can be switched is approximately 600 Hz. Faster, software compatible processors are available which can boost this rate to approximately 1.8 KHz for general waveform synthesis requirements. For d.c.-to-d.c. conversion synthesis requirements for two terminal diagonally connected MHD generators, which are much less general in their real-time speed requirements than Faraday connected generators, it is possible to go to at least 50 KHz rates with the proper control microprocessor. However, GTO duty cycle limitations along with switching and transformer core losses will generally limit such rates to below 10 KHz.

3.3.1.2   Virtually any waveform requirement within reason can be successfully generated using the PASC technology. For highly non-linear loads or loads requiring sophisticated startup and shutdown cycles, closed-loop feedback control of the switching algorithm will in general be required. Output circuitry inverter design must be used if continuous mono-polarity d.c. pulse waveforms are to be generated, because transformers are fundamentally bipolar devices.

3.3.1.3   The efficiency requirements for snubbing or shorting in order to push the energy out the transformer(s) into the load become more severe as the step-up turns ratio becomes high. To achieve maximum efficiency, it may be necessary to use capacitive snubbing or shorting, particularly if the connected load is highly inductive in nature. Such a requirement is much less severe for d.c.-to-d.c. switched mode voltage conversion operation.

3.4 Feasibility Demonstration Test results obtained using intermediate-level power semiconductors.

Following the original Feasibility Demonstration tests which were conducted in August of 1989, high-power, symmetric GTOs rated at plus-or-minus 1200 volts and 80 amperes were ordered to refit the 16 power injection lines, and 16 high-power natural-commutation thyristors to be used as snubbers. Delivery on these units was delayed twice by the vendor until November 1989, with final refitting being finished in December. It was thought that the 16 asymmetric, low-power snubbing GTOs could be replaced with high-power natural-commutation thyristor units, since the snubbers should be self-extinguishing in steady-state, periodic operation. Testing revealed however, that unless the transient was very well behaved (less than ninety milliamps of current), these snubbers would lock up with resultant incorrect and damaging performance. Hence the 16 asymmetric, low-power snubbing GTOs were put back into operation because it was thought that in steady-state operation they would be of sufficient size to permit operation of the Demonstration system at full power (input injection resistance of 2.5 ohms minimum), and because of the long delay in getting more units (we in fact could not get any vendor to commit to a guaranteed delivery schedule for more of the high-power units). This long delivery schedule is particularly true of symmetric voltage capability GTO units; asymmetric units in which the voltage standoff in the reverse bias mode is very low are more readily available because of there usage in motor control systems where the incorporation of a series blocking diode with the attendant higher circuit loss is considered to be less important than the reduction in cost of the GTO.

Figures 13 through 20 show data obtained during intermediate level power runs during February and March 1990, with the power supplies set at 120 vdc source voltages. Source resistance values of 10 and 2.5 ohms for loads of 10 and 100 ohms were employed to obtain these output waveforms. Both step-up and step-down transformer connections were tested and the results are indicated.
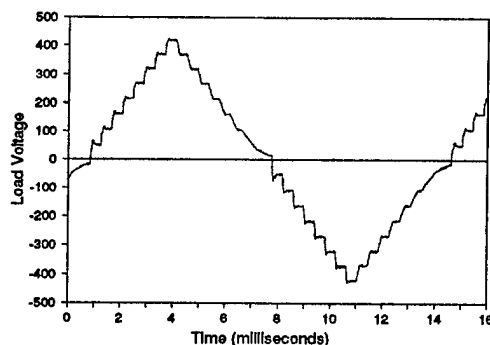
Figure 13. Load voltage for 2.5 ohm source impedance and 100 ohm load impedance for step-down transformer connection.

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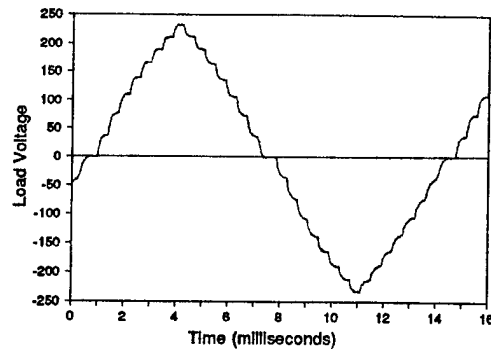
Figure 14. Load voltage for 2.5 ohm source impedance and 10 ohm load impedance for step-down transformer connection.
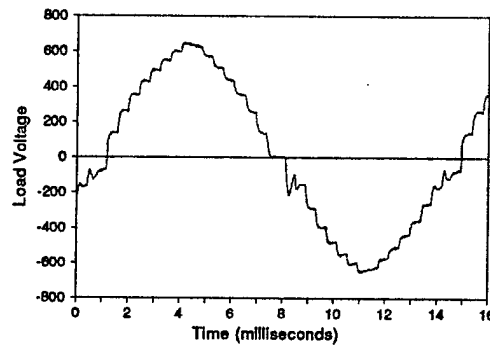
Figure 15. Load voltage for 2.5 ohm source impedance and 100 ohm load impedance for step-up transformer connection.
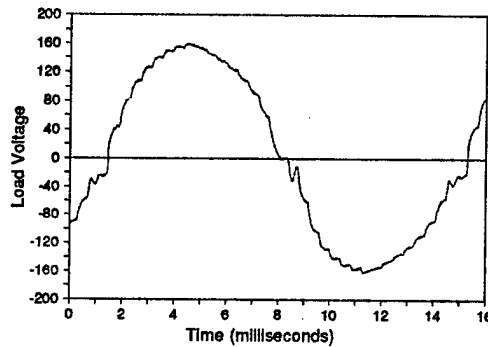
Figure 16. Load voltage for 2.5 ohm source impedance and 10 ohm load impedance for step-up transformer connection.

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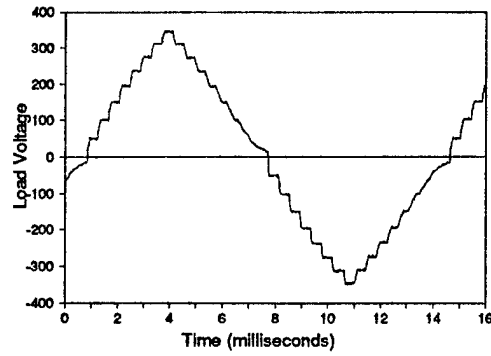
Figure 17. Load voltage for 10 ohm source impedance and 100 ohm load impedance for step-down transformer connection.
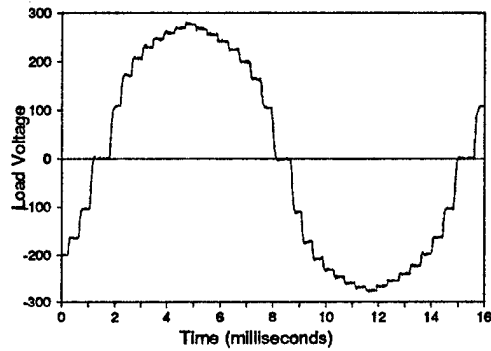
Figure 18. Load voltage for 10 ohm source impedance and 100 ohm load impedance for step-up transformer connection.
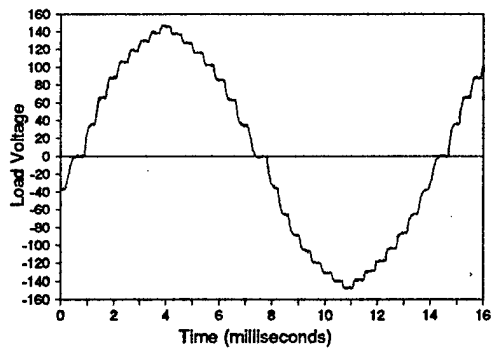
Figure 19. Load voltage for 10 ohm source impedance and 10 ohm load impedance for step-down transformer connection.
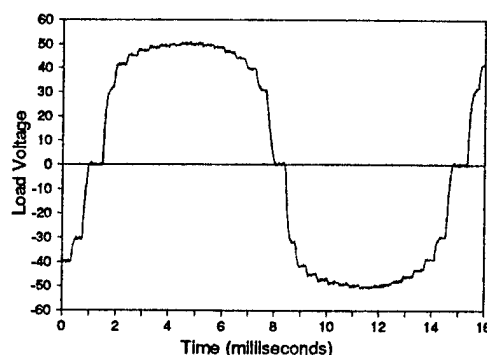
Figure 20. Load voltage for 10 ohm source impedance and 10 ohm load impedance for step-up transformer connection.

The output voltage data scales by a factor of two the data collected using the 60 vdc sources used in the low-power Feasibility Demonstration testing results obtained during August 1989, discussed above in section 3.3. The general characteristics of the results obtained during February 1990 are similar to those obtained previously with the following additional comments:

a. The low-power GTO snubbing units are being used at or beyond their maximum ratings, especially with respect to maximum current; this produces the anomalies shown in Figures 15 and 16 where two snubbers GTOs are not working properly. It can be seen that snubber number zero (very positive peak of the waveform), and number eight (right after the waveform goes negative), are malfunctioning. It was ascertained that snubber zero had completely failed. In the case of snubber eight it was determined that it is partially failing. After replacement the tests were repeated with the same snubbers again failing after a very short interval. It must be emphasized that these tests were taken beyond the safe operating ratings of the snubber GTOs. The source resistors also became too hot to touch within five seconds of the start of these tests so that protracted experimentation evaluation of these anomalies as well as reducing the source impedances to zero were not consdidered to be prudent.

b. In general the results for step-down transformer connection for the intermediate level power tests are better than for step-up connection. This agrees closely with that already obtained in the low-power demonstration tests. The output waveforms are also better for large load impedances than for low load impedances. Again this agrees closely with previously results and is logically explainable using the exact same argument as given in section 3.2 for the diagonal generator simulation results.

c. Because of the extreme sensitivity of the tests to failure of the low power GTO snubbers, intermediate-level power data of non-sinusoidal waveforms was not attempted.

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3.5 Description of some preliminary harmonic suppresion control waveform algorithms and a new data acquisition system and control system.

3.5.1 Introduction

A question of significant interest in the application of the PASC principle to commercial power production is whether a digitally generated sinusoidal waveform approximation may be controlled in such a fashion as to minimize the higher harmonic content of the synthesized output. In this section we present an application of the Internal Model Principle of feedback control whereby a closed-loop system incorporates an "internal model" of a known reference input for robust tracking of the reference and for improved disturbance rejection. Applying this strategy to a Pulse Amplitude Synthesis and Control (PASC) system requires tracking a sinusoidal reference with minimal error while simultaneously observing other performance measures and design constraints. An inherent feature of a PASC system is the discrete switching of sources to form the pulsed wave. To this end, it is natural to consider a discrete-time control algorithm in which parameters can be easily changed and source switch points are directly available in binary at the output of the controller. The development of the discrete-time Internal Model principle follows closely the continuous-time case given by Francis and Wonham in [4].

In what follows, the Internal Model principle is first introduced. A continuous-time system is then built and tested to demonstrate the validity of the model. The closed-loop system is then discretized and a nonlinearity is added at the input to the discrete plant to represent the switching action of the PASC system. Design considerations are then discussed and some generalizations are made about the control action to be applied. The system is then simulated and analyzed for tracking and harmonic content. Finally, conclusions are drawn and suggestions made for directions in further work.

3.5.2 The Internal Model Principle

The Internal Model principle of control theory states that a "structurally stable" design always incorporates a model of the reference to be input and a model of the disturbance to be rejected in the feedback path. Francis and Wonham [4] give a general proof of this principle and Franklin and Powell [5] apply the principle to a number of different signals including a sinusoidal reference. Perhaps the most convincing examples of the principle can be found in elementary control theory. It is well known that a Type I system can track a step input with zero steady state error. Type I systems are easily recognizable in that they contain a single pure integrator. In the sense of the Internal Model principle, however, a pure integrator is a model of a step input. Similarly, a Type II system contains a model of a ramp input or a double integrator. Francis and Wonham prove that an extension can be made to the general case in which the input is an arbitrary function of time. One only needs to find a model of the input in order to be able to track it. It would seem natural that the extension to the sinusoidal reference input case could be modeled by an oscillator at the frequency of the sinusoid. In fact, Franklin and Powell show that this is true. The internal model of a sinusoidal reference is shown in Figure 21.

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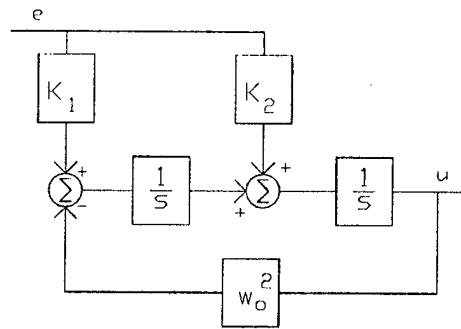
Figure 21. Internal Model of Sinusoidal Reference

Practical experience and testing have shown that a reasonable model for the PASC system under certain operating conditions is simply a single, two-winding transformer with an n-step "staircase" source. If that staircase source is modulated so as to produce an uncontrolled output such as shown in Figure 25, from a simulation standpoint the model is equivalent to using a set of four separate transformer each having two primary windings and a single secondary with all of the secondaries connected in series. This second realization of a four pulse PASC system is of course the way the system must actually be realized in practice because of the voltage leakage principle. The range of valid applicability for this model is low frequency operation in the linear region of the transformer B-H curve and uniform, time-invariant dc source voltages. This is the simplified model chosen to represent the plant for the development of the control strategy. Values for inductance and resistance used in the model are actual test results from the transformers in use in the PASC system. The transformer model is shown in Figure 22.
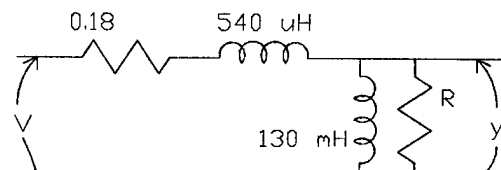
Figure 22. Transformer model for simulation

For further simplification, the transformer turns ratio is taken to be 1:1. The transfer function, G(s), representing the transformer can be easily found in the s-plane to be,

$$G(s) = \frac{1851.85Rs}{s^2 + (1859.54R + 333.33)s + 2564.1R}$$

The load resistance, R, is left as a parameter which can be varied to perturb the system when the controller is implemented.

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3.5.3 The Continuous-Time System

Figure 23 shows the continuous-time closed-loop system. The switching non-linearity is represented by the "staircase" in the nonlinear block. The basic function of the nonlinear block is to quantize the control input. This nonlinearity reflects the requirement that only an integer number of dc sources be active at any one time.
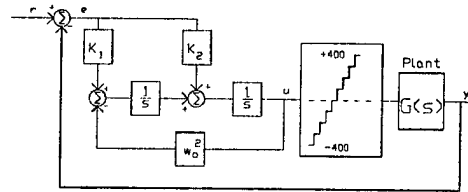
Figure 23. Closed-Loop System

3.5.4 Discretization of the System

As was mentioned earlier, it is desirable to use a digital controller in this application. This section presents a discretization of the closed-loop continuous system shown in Figure 23.

3.5.4.1 The Internal Model

The transfer function of the internal model as shown in Figure 21 is

$$C(s) = \frac{K_1 + sK_2}{s^2 + \omega_o^2}.$$

This equation can be split into two parts and easily converted to the Z-domain by table look-up. The discrete transfer function of the controller is then

$$C(z) = \frac{K_2 + \left(\frac{K_1}{\omega_o} SIN(\omega_o T) - K_2 COS(\omega_o T) \right) z^{-1}}{1 - 2 COS(\omega_o T) z^{-1} + z^{-2}}.$$

Since the switching nonlinearity can be easily represented digitally for simulation purposes, a zero-order hold was placed at the input to the plant after the nonlinearity as shown in Figure 24. Again, obtaining the discrete equivalent of the s-plane transfer function is straightforward and can be accomplished by table look-up methods. The z-plane transfer function of the plant and zero-order hold is

$$G(z) = \frac{1851.85R}{p_1 - p_2} \frac{(e^{-p_2 T} - e^{-p_1 T})(z^{-1} - z^{-2})}{1 - (e^{-p_1 T} + e^{-p_2 T})z^{-1} + e^{-(p_1 + p_2)T} z^{-2}}$$

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where p_1 and p_2 are the roots of the denominator polynomial of $G(s)$ and are a function of R.

3.5.4.2   The Discrete-Time System

We now have enough information to build the discrete-time system shown in Figure 24.
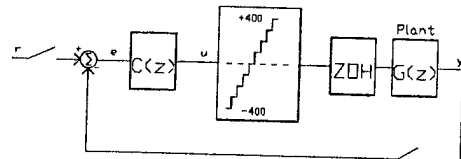
Figure 24. The Discrete-Time System

The system of Figure 24 was tested in various configurations for verification of model parameters using the simulation routines in MATLAB. The results were reasonable representations of the physical system. A case is shown in Figure 25 where the reference input is a 60 Hz sinusoid with a peak amplitude of 400 volts. The load resistance is 100 ohms. Results from the open-loop configuration are shown on the same graph, but are almost indistinguishable from the closed-loop with the controller gains both set at 10^{-2}. More simulations are shown in the following sections.
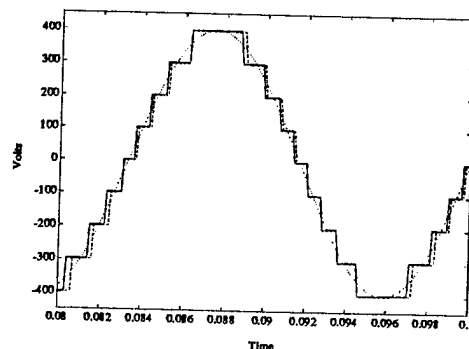
Figure 25. Model and Controller Test

3.5.4.3 Design Considerations

Numerous system constraints and performance objectives make it difficult to determine the appropriate gains for the controller. For the purposes of this paper, two performance objectives are considered to be of primary interest. The output should track the reference sinusoid with minimal phase lag and should contain a minimal total harmonic content. The PASC system should have the ability to supply or consume reactive power (VARS) when connected to an external network such as a power system. This would be accomplished by setting the reference phase leading or lagging with respect to the network voltage. This is the reason for the importance of tracking the reference with minimal error. The reason for the minimal harmonic content criterion is obvious. In a specific application, there may be many more performance criterion with equal importance.

An important system constraint is the finite switching time required to trigger and commutate a GTO switch. A reasonable estimate of the time required to bring a GTO to full conduction and subsequently commutate it is approximately 20 μS. For this reason, the sampling rate has been kept at 100 μS or greater throughout the simulations. With these in mind, two root loci were constructed in the s-plane to get a feel for the effect of controller gains on the system. The nonlinear block was not included in the open-loop transfer function used to obtain the root locus. The first root locus is shown in Figure 26. In this case, k_2 is zero and the root locus is constructed on k_1.
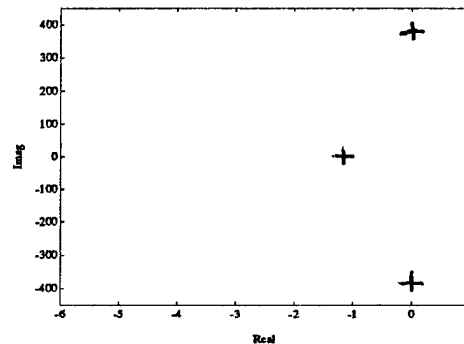
Figure 26. Root Locus on k_1

From Figure 26, it is seen that it is extremely hard for k_1 to move the oscillatory poles off of the $j\omega$ axis. This is understandable by looking at Figure 23 and noticing that with $k_2=0$, k_1 is feeding a pure oscillator. Figure 27 shows a root locus on k_2. Here it can be seen that significant damping can be added to the system while keeping the poles at the same oscillatory frequency. Both loci were constructed using 100 gain points between 0.1 and 10.

28
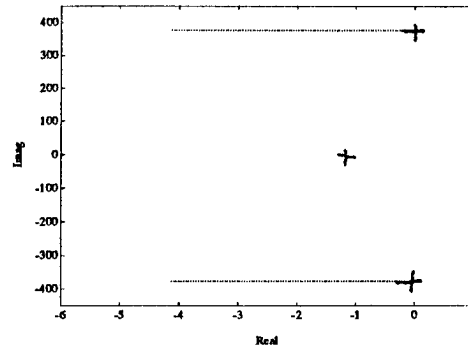
Figure 27. Root Locus on k_2

It will become evident that increasing k_2 increases the number of switching actions per ac cycle as the controller trys to track the sinusoid perfectly. This action would fatigue the switches and increase the high frequency content of the output if carried to an extreme. An optimal choice for the gain settings would be difficult to calculate under the physical constraints of the system. Simulations will give a better feel for the choice of gain, but the root loci have shown that k_2 has a much greater effect on the system closed-loop poles than does k_1.

3.5.5 Simulations

Figures 28 and 29 show the effect of increasing the k_2 gain. In Figure 28, $k_2=1$ whereas in Figure 29, $k_2=10$. In both cases, R=100.
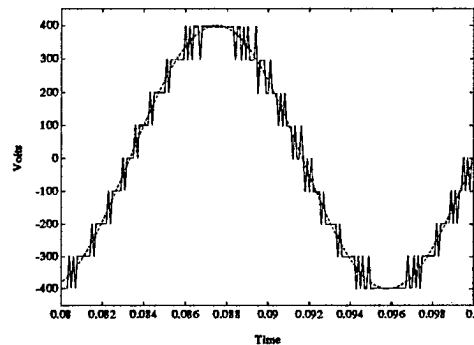
Figure 28. R=100, $k_1=1$, $k_2=1$

29
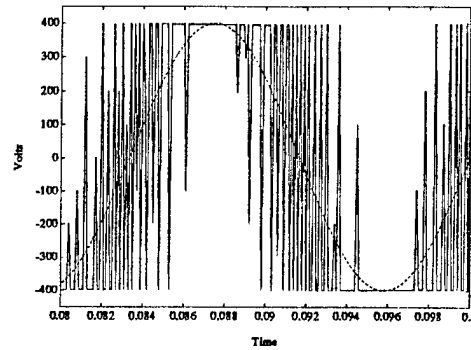
Figure 29. R=100, k_1=1, k_2=10

Figure 30 shows the spectrum of Figure 28 against the spectrum of the uncontrolled plant. The higher frequencies are conspicuous here.
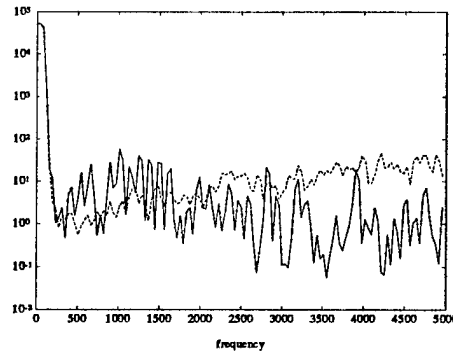
Figure 30. Spectrum of Figure 28

To illustrate heavy loading conditions where the inductance of the transformer starts to become significant, a simulation was made for R=1. Figure 31 shows the outputs of the controlled and open-loop systems with respect to the reference input. Figure 32 shows the spectrum of Figure 30.
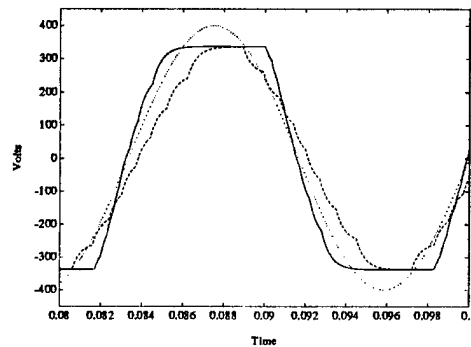
Figure 31. R=1, k_1=1, k_2=0.1

30
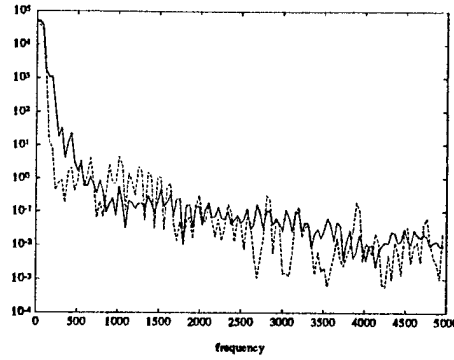
Figure 32. Spectrum of Figure 30

In a third case, the frequency is increased to 600 Hz. Figure 33 shows the output and Figure 34 shows the spectrum.
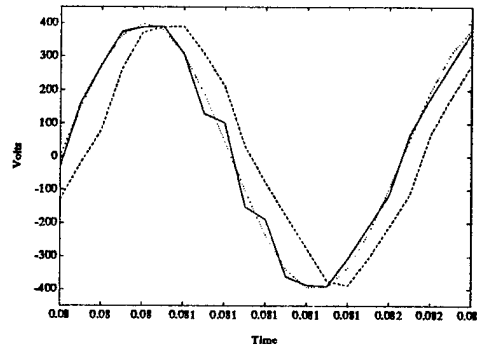
Figure 33. F=600 Hz, R=10, k_1=1, k_2=1
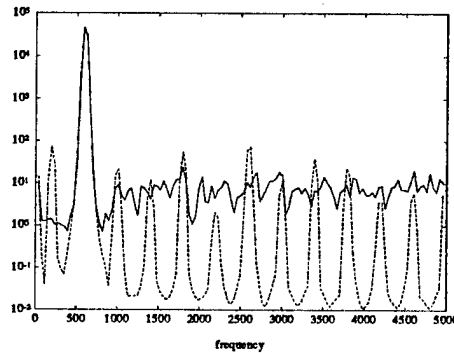
Figure 34. Spectrum of Figure 33

Numerous other simulations were conducted among which were cases where the reference frequency was not equal to the controllers ω_o. Extreme attenuation of the output was experienced in these cases where the internal model was no longer a model of the input.

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3.5.6 Conclusions

The Internal Model principle has been examined and applied to a system with which we would like to track a sinusoidal reference input. The principle is summarized by Francis in saying, "...a structurally stable synthesis must utilize feedback of the regulated variable, and incorporate in the feedback path a suitably reduplicated model of the dynamic structure of the disturbance and reference signals." [4]. The development of the model for a sinusoidal reference followed from the work in [4] and from a discussion in [5, p.389]. The continuous-time model was discretized and the discrete system was run through simulations and analyzed for spectral content.

While it is clear that the controlled system tracked the reference input better than the open-loop system in all cases, it is not clear that significant reductions in harmonic content occurred in all cases. At low frequency and low loading conditions, there is a trade-off between low frequency harmonic content and high frequency content in the controlled case. More control provides lower harmonic content below about 600 Hz, but increases then content of the spectrum above 600 Hz. This may suggest an optimal gain for a given loading condition to minimize total harmonics. It may be the case, however, that high frequency harmonics are filtered adequately by the external system or that the cost of filters is much lower at high frequencies and one would simply want to reduce the amplitude of the lower part of the spectrum at the expense of faster switching.

3.5.7 The Harris Design Contest Controller

Early in 1990 the Harris Design Contest was announced. This contest provided a small prototype board to the contestants containing a very high speed control processor chip directly programmable in the FORTH higher level language, a real-time event clock, and with additional space on the board to place additional memory and an analog-to-digital converter. Two of our graduate students entered this contest with the objective of replacing our Feasibility Demonstration Microvax/KXT-11 controller with the Harris board and implementing the internal model controller. From a power/weight ratio measure this promised some improvements. Prior to this the Feasibility Demonstration system was controlled only in the open-loop using a DEC MicroVax II hosting a DEC KXT-11 (PDP-11 based) single board computer. This system was adopted because it allowed software development at maximum speed by permitting implementation of the control sequence algorithm in a higher order language. In this case, the "open-loop" consisted of downloading a pre-programmed switching schedule developed on the Microvax using a cross-compiller, to the KXT-11 and iteratively running the schedule to produce an output waveform. A cumbersome limitation of the KXT-11 processor is that all timing of events was limited to a multiple of the basic instruction cycle, (a real-time event timing clock along with interrupt driven scheduling of switching would aleviate this problem in a production system, but at the expense of greater software design effort). By using the Harris board several improvements in PASC controller design and operation appered possible. New routines and switching schedules could be developed with any ASCI file editor on a PC and down-loaded directly into the Harris board for direct execution without the necessity for the normal compiller software iteration sequence. To test compatibility of the RTX 2001A with the existing hardware, an open-loop switching schedule was written for the RTX. FORTH programming on the RTX 2001A proved to be fast and efficient in comparison, particularly with respect to

the ASIC bus output. Other drawbacks of the DEC controller sequence program chosen, (again dictated because of the development time constraints necessary in meeting the original Feasibility Demonstation tests), included the inability to control phase, amplitude, and/or frequency on-line, the inability to compensate for dynamic loading, and the inability to adjust the switching schedule to achieve a secondary goal such as harmonic minimization or component failure. The RTXEB provided for the Harris Design Contest had the potential ability to deliver all of these things as well as the ability to work in parallel with other boards as would be required in a three-phase system.

3.5.8   The Digital Controller

With the design goal as stated above, i.e. the synthesis of a 60 hertz sinusoid with minimal harmonic content, the controller design was centered around the internal model principle of control theory. Simply put, the theory states that in order to track a reference exactly or to reject a disturbance completely, a model of the reference/disturbance must be incorporated in the feedback path of the controller [4]. In the application proposed for the Harris Design Contest, the authors wished to track a reference sinusoid. The internal model principle dictates that a sinusoidal oscillator must be incorporated in the feedback loop. The closed-loop system can therefore be represented in continuous time as in Figure 35.

The non-linearity resembling a staircase represents the discrete levels of output voltage available. The number of steps corresponds to the number of transformers connected to form the additive waveform. To implement the controller on the RTX 2001A, the discrete-time equivalent of the oscillator in Figure 35 was developed and written in the form of a digital filter. As a ratio of polynomials in z^{-1}, the filter can be written

$$C(z) = \frac{K_2 + \left(\frac{K_1}{\omega_o} SIN(\omega_o T) - K_2 COS(\omega_o T) \right) z^{-1}}{1 - 2 COS(\omega_o T) z^{-1} + z^{-2}}$$

where z^{-1} is the discrete delay operator. It can be shown that effective control for this application can be achieved by setting $K_1 = 0$. The software implementation of the filter is carried out using transposed direct form II. Figure 36 shows the closed-loop system in block diagram form as it is operating on the RTX 2001A.
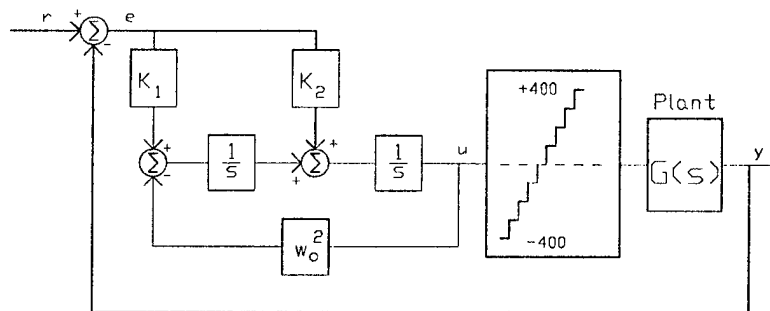
Figure 35. The closed-loop system in continuous time.
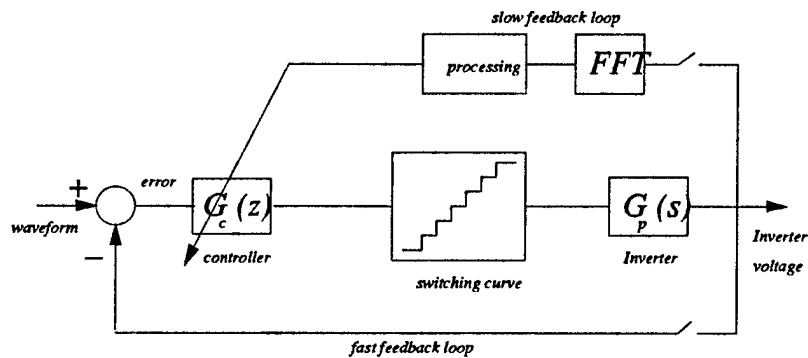
Figure 36. Block diagram of closed-loop system.

3.5.9 The Continuous Fourier Transform

The action of the controller was first studied using the MATLAB software packages before the actual implementation on the system. The results of the simulations confirmed an intuitive guess that increasing the gain of the controller would force the output to track the reference sinusoid more closely thereby reducing the lower harmonics at the expense of more frequent switching actions. The increase in the amount of switching required to track one cycle of the reference leads to an increase in the higher harmonics contained in the output, thus a tradeoff exists between reducing the lower harmonics and the higher harmonics. The definitions of lower and higher order harmonics is purely subjective. For the commercial utility application, it is always desirable to reduce the lower harmonics because the higher harmonics tend to attenuate rapidly along a power transmission line or through a power transformer.

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With this in mind, it was suggested that a means be found to monitor the harmonic content of the output and increase the controller gain to a point where the higher order harmonics stay within a reasonable limit and there is no damage to the GTOs by attempting to switch too fast. The continuous Fourier transform outlined in the Harris publication RTXpress [6] proved to be an answer to the problem and the ease with which interrupts are handled on the RTX 2001A made implementation of this feature extremely simple. One CFT is performed on the output at 180 hertz (the third harmonic) and another is performed at 720 hertz (the twelfth harmonic). A ratio of the third over the twelfth is then formed and this ratio is used in a form of adaptive control to adjust the gain of the controller. As the ratio increases, we wish to increase the gain to bring the ratio back down to a relatively constant value which experience has shown to be governed by physical limitations on the switching speed of the GTO's. The CFT's are performed in the background of the normal controller action and are continually being interrupted to perform the control by an on-board timer provided on the RTX 2001A. This process is discussed more thoroughly in the section on software implementation.

3.5.10 Hardware Interface With the Existing System

The system, as it was constructed for the Microvax realization, utilized 32 TriState drivers, each one driving a single gate firing circuit through an optical isolator. The 16 data lines were multiplexed using a 3 bit address into the 32 GTO gate firing circuits. The simple multiplexing scheme consisted of one address bit dedicated to " output enable " for supervisory control and the remaining two bits were used as TriState latches to toggle the information into either of two sets of 16 TriStates. This system provides for positive latching of information into the gate firing circuits and provides more speed than will ever be required of the GTOs.

The ASIC bus architecture on the RTX 2001A made the interface to the existing system as easy as could be imagined. The 16 GD data lines are brought directly to the existing TriStates. The output enable bit is held low by means of a toggle switch installed in the prototype area of the RTXEB. The GIO bar and the GR/W bar are inverted and ANDed with the GA0 ASIC bus address line. The result of this operation becomes one of the TriState latches while the GA1 line ANDed with the same two " data valid " lines gives the other latch. This leaves one of the 3 external ASIC bus address lines to be used as a Start of Conversion signal to the A/D converter. Figure 37 shows the chip layout on the RTXEB while Figure 38 shows the logic just described.
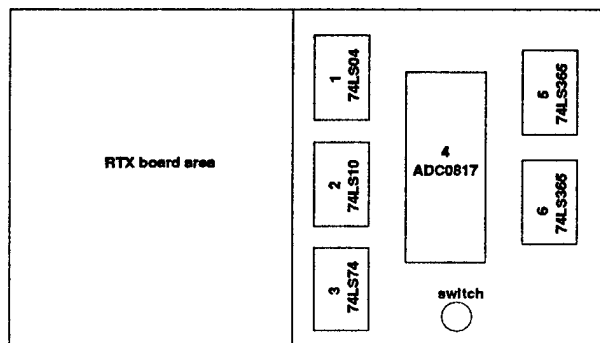
Figure 37. Chip layout on RTXEB.

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Figure 38. Logic diagram for Mux.

The A/D converter used in the contest application is an 8 bit device running on an independent 1 Mhz clock. Figure 39 shows the clock design as well as the pinout for the A/D. Data from the A/D is brought in through the bi-directional GD data lines to the ASIC bus. The A/D is given a Start of Conversion command at each controller time step. The simplest practical method to achieve this is to give the A/D a Start of Conversion signal at each read. This is accomplished with a monostable (one-shot) multivibrator. The one-shot is toggled in the same manner as the TriState latches with the GIO bar, GR/W bar, and the GA2 ASIC bus external address line. The GIO bar is inverted and ANDed with the GR/W bar and the GA2 lines. This provides the digital controller with feedback containing at most a single time-step delay. The A/D analog data is fed to the board by a standard voltage transducer. The output of the transducer is given a dc offset and is passed through a 2:1 resistive divider located on the RTXEB.

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Figure 39. A/D pinout and external clock.

The ASIC bus and GD data lines proved to be extremely easy to work with and minimal time was spend on hardware interfaces. The 3 GA address lines provided give the freedom to multiplex to a greater number of GTOs as would be the case in a system containing more numerous dc sources. In the present configuration, the RTXEB hardware could potentially drive 64 isolated dc sources which is a reasonable number for commercial applications.

3.5.11 Software Implementation

The software design strategy for the RTX Design Contest was to implement controller action using vectored interrupts and to run any peripheral processes secondary to the controller. The on-board timers furnished on the RTX 2001A provided the ideal solution to the controller problem. Since the timers decrement once for each clock cycle, the calculations to determine the timer preset value corresponding to a desired sample rate are simple. The control algorithm is then carried out by loading a timer preset register with a pre-calculated value, unmask the timer, and execute the digital filter at each interrupt. The RTX 2001A timers send an interrupt upon reaching a value of zero and subsequently clear the interrupt and reload to the preset value. To reduce stress on the GTO's, an upper limit of 10 Khz sampling rate was placed on the controller. In an extreme case, this would allow the GTO 100 μseconds to move into conduction before it could receive a commutation signal to stop conduction. At the 8 Mhz clock rate, 10 Khz sampling corresponds to a preset value of 800.

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3.5.12 The Sampling Period and Controller Interrupts

For reasons of simplicity, the sampling rate was chosen to be 2 Khz or a preset value of 4000. This rate allows a CFT to be performed at two frequencies between each interrupt. A more optimal strategy which will be easily implemented on the RTX in the near future would be to double the sampling rate to 4 Khz and perform a single CFT between each interrupt. The mode of operation for the Harris Design Contest was chosen so that testing of the prototype could be carried out in a reasonable amount of time and with a significant margin of safety.

The steps involved in handling an interrupt vector corresponding to an execution of the digital filter is shown by the rightmost flowchart in Figure 40. A value for the reference sinusoid is obtained from a data table located in the RTX 2001A data memory. The table is filled with 200 8 bit points corresponding to 8 bit values of the first quarter of a sine wave. A pointer points to one of 800 values on a hypothetical sine curve. If the pointer lands in any quadrant of the curve other than the first, a routine called SIN negates a corresponding value in the table or "folds" it or both, depending on what quadrant the pointer is pointing to. In this manner, the number of data points required to fill the table is reduced to one quarter of the number required to represent a full sine period. A table look-up approach was used to determine the values of the reference sinusiod as opposed to direct calculations due to the increased speed of execution of the look-up method.

After the reference point is obtained, a value is retrieved from the A/D converter. This value is scaled and subtracted from the reference to form the error signal shown in Figure 36. At this time, the A/D value is also stored in a table to be used in the CFT. The digital filter is then executed. The output of the digital filter is the theoretical value to be input into a linear system. Since the system being controlled contains the "staircase" non-linearity, the digital filter output must be quantized before being sent to the TriState drivers. The routine called OUTWORD performs the function of quantizing the filter output and sending the quantized value to the GD data lines via the ASIC bus. OUTWORD quantizes the filter output so as to equally load the dc sources under normal operating conditions as best as possible. Control is then returned to the interrupted procedure. The interrupt handler takes about 800 clock cycles to complete.

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Main Routine

START

enable timer interrupt

Is data valid? — yes → FFT

no

FFT

analyze

update controller gain

key pressed? — yes → disable interrupt

no

disable interrupt → END

Interrupt Routine

START

generate point on waveform

get A/D value

waveform value - A/D value

apply controller (digital filter)

staircase limit for switches

pulse switches

RETURN
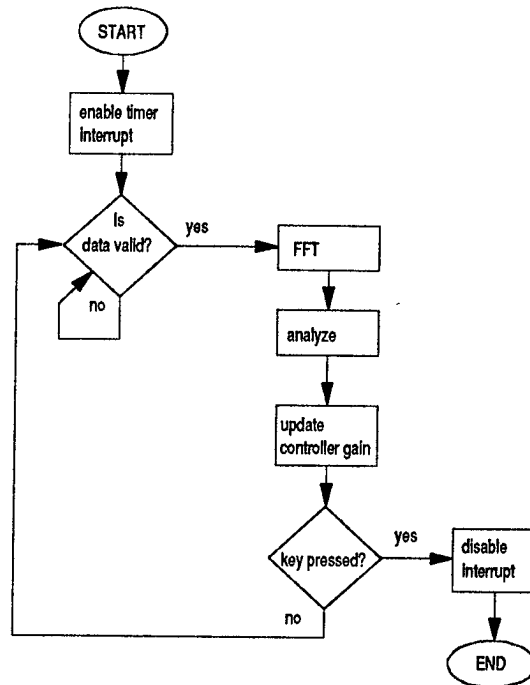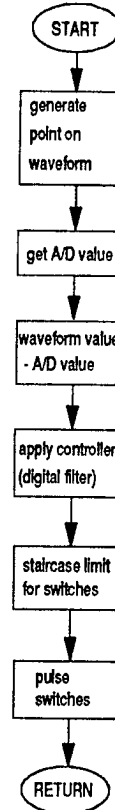
Figure 40. CFT and Interrupt flowcharts.

3.5.13 The CFT

The CFT is performed continuously in a BEGIN ... AGAIN structure and is interrupted at each controller time step by an on-board timer. The CFT also contains a keyboard check. Any keystroke caught while in the process of running the inverter will cause a call to a shutdown routine. This routine masks the interrupts, opens all GTOs, and quits the BEGIN ... AGAIN loop to enter the interpret state on the RTX 2001A. Assuming no keystroke was caught and following the procedure outlined in RTXpress [6], the most recent A/D value is

retrieved from the CFT table located in data memory. This is a circular table, so the oldest A/D value is found just above the most recent in memory. This value is also picked up with adjustments for foldover and subtracted from the most recent. This quantity forms the [f(k) - f(k-N)] quantity which multiplies the exponential. The exponential is broken up into its real and imaginary parts and evaluated using Euler's relation as a cosine and sine. The values of the cosine and sine are picked up from the sine table used in the controller algorithm. The resulting real and imaginary parts of the recursive CFT are squared and added. The square root of this quantity is the magnitude of the CFT. This procedure is performed twice, once at each of two frequencies.

The two frequencies which were determined to be indicators of "lower" and "higher" harmonics for this application are 180 hertz and 720 hertz. A ratio is formed from the magnitudes of the CFT at each of these frequencies and this ratio is used to determine any adjustment needed to the controller gain. Safety features included in the CFT are a flag to indicate that new data is available in the CFT table. This flag prevents the CFT from performing calculations on the same set of data repeatedly. An overflow flag is also included in the squaring operations. If an overflow is detected at this point, the CFT is re-initialized and waits for the CFT table to completely fill up before a new calculation is started. There are many options available to improve the performance of the CFT. Some of these are discussed in the conclusions. As implemented here, the full CFT takes about 2000 clock cycles to complete.

3.5.14 Memory Allocation

The philosophy behind the memory allocation on the RTXEB was to first design the controller and CFT to determine how much memory was needed for code space. This being done, most of the rest of the available memory could be used for data. Two data tables are needed in the design. A 200 point sine reference table provides as much accuracy as is being retrieved from the A/D. This leaves enough room in memory for a 1000 point CFT table. Figure 41 shows a map of the RTXEB SRAM available and how it is allocated in the design.
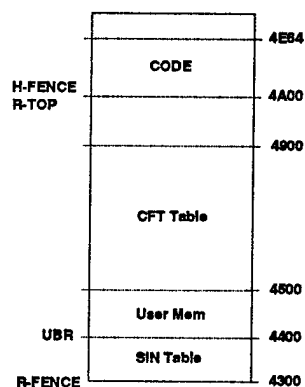
Figure 41. Memory map.

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3.5.15 Conclusions and Discussion

The Harris RTX 2001A proved to be much easier to work with than had been anticipated. As novice FORTH users, the project was approached with a certain degree of apprehension. Features that made the board easy to work with from a programming viewpoint are the on-chip compiler and the UART provided as development software. Architecturally, the speed with which operations can be performed with astute programming on the dual stacks is rewarding. As the software development progresses, one can continually find faster ways to accomplish things that look at first like they are already optimal. I/O on the RTXEB also proved to be trivial.

Another feature of the RTX 2001A that was found to be extremely useful in this application was the use of the 32 user memory variables addressed by the User Base Register. Using these variables and addressing them by their literal values cut the execution time of both the filter and the CFT to at least one third of the original time.

Closing the loop in the control of the prototype static inverter represents a significant improvement in this technology. Future developments are now possible in the areas of interactively changing the shape, phase, frequency, amplitude, and harmonic content of the output waveform. Dynamically changing loading conditions are handled extremely well within a reasonable range with the controller described in the paper. The five external interrupt lines provided on the RTX 2001A would make it easy to implement any or all of the features described above. It would seem most feasible at this stage that a graphically oriented software package would be developed to communicate with an operator and the external interrupts would change parameters in the control algorithm accordingly.

3.6 Final calculation results for a space-deployed minimum power-to-weight ratio PASC system at a 100 MWe level.

In response to a desire for a determination of the power-to-weight ratio for the PASC technology at a nominal 100 MWe size, the contractor has supplied previously an estimate for this information. The assumptions and details of the calculation were covered in the April 1989 - Sept 1989 Technical Progress Report. In particular, the source MHD system to which it is assumed, the PASC system would be connected is defined as:

Source MHD diagonal terminal voltage at rated current = 1700 volts dc.

Rated source total diagonal current = 62,700 amperes dc

Desired PASC secondary voltage = approximately 100 Kv dc.

Additional work in changing the controller to only one or more single board computers (SBC), from the present Feasibility Demonstration system Microvax II with KXT-11 SBC, as discussed above in section 3.5 on the data acquisition and control system, indicates that the power-to-weight conversion ratio can be improved by approximately 200 pounds by the incorporation of such a system. For purposes of completeness we repeat below the basic system design assumptions.

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3.6.1 Basic Assumptions Used In The Power-to-weight Ratio Calculation

The value obtained for a weight estimate of the PASC or any technology is highly dependent upon the assumptions made in the design, especially since a full scale detailed system design does not exist. We have assumed the following:

a. There is a reasonable amount of liquid hydrogen around for cooling of the transformer conductors, core, and GTO heat sinks. Since a two-terminal diagonal MHD generator is assumed as a source, and the GTO thyristors can be paralleled together to handle the high primary current of the generator, only two distributed plate heat sinks will be required which may be cooled by liquid hydrogen conduction cooling and circulation. A detailed calculation of how much hydrogen would be gassified in vaporization has not been done but it does not appear to be excessive for a 600 second mission. With this assumption, the resulting design is conservative i.e., the resulting design is a steady state design.

b. It is assumed that the desired output voltage is nominally 100 Kv d.c. We have included the weight of a generic full wave d.c. rectifier following the PASC system in the calculation although its design will depend somewhat on the required weapons system internal impedance and loading characteristics. However, for simple resistive or leading power factor loads the requirements of such a rectifier will be very simple, requiring no large filtering capacitor, since the PASC system would be programmed in a standard d.c.-to-d.c. square wave switching mode which results inherently in almost no ripple in d.c. output. This is especially true if the design switching frequency is high. Clever heat sink design will be required because of isolation requirements. Based upon a load current of 1000 d.c. amperes, the total weight for such a rectifier should be less than 500 kilograms.

c. In view of b., and because transformer weight reduction results with increasing operational frequency, it is desirable to seek a high frequency design. The upper frequency of operation will be limited either by GTO minimum timing limitations or by the GTO switching transition losses. Because of the increasing relative efficiency of large GTO thyristor units together with assumed high frequency of operation, only a single phase inverter will be necessary, which will limit the gate switching component count.

d. In a d.c.-to-d.c. switched design, such as contemplated here, the control computer speed requirements are very easily realized even up to switching frequencies of 50 KHz, because no complex waveform synthesis is required and all of the switching gates are multiplexed in parallel either in a positive or negative polarity grouping. The gate switching interface design must however, be carefully done since relatively large amounts of gate switching power must be accommodated in parallel at high frequencies and even symmetric current loading of the GTO thyristors must be accomplished.

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In the discussions which follow, the design considerations have been divided into two main areas: the design of the PASC switching matrix, and design of the PASC transformer.

The PASC switching matrix is assumed to be on a common ground heat sink located at the exhaust potential of the diagonally connected generator energy source. Careful design must be done to balance symmetrically the large diagonal current between approximately forty 2000 ampere, 4000 volt GTO gates. The design of the PASC transformer, since it is the largest contributor to the PASC system mass, is now considered in detail.

3.6.2 Design of the PASC Transformer

The conversion of energy in the PASC transformer will have a significant effect upon the performance and efficiency of the resulting PASC system. There are many interacting design parameters in a transformer and each has an important influence on overall system weight, efficiency and cost. Because of these parameter interdependences, there are many trade-offs to consider in achieving design optimization. Time and funding limitations permit only a first pass estimate of an such a optimized design. Again, the specific details of the calculation are given in referenced report cited previously.

3.6.3 Final Design Transformer Loss Calculation

After the selection of Supermendur as the transformer core material of choice, a simple core transformer design was assumed using 0.002" laminations. As described above, a program to compare Supermendur designs at different frequencies, wire sizes, and dimensions was constructed and run. Because of Supermendur's high saturation point, it can operate at 1.5 Tesla peak flux densities at higher frequencies with small core losses relative to other known materials. Beginning core configurations had lengths of 160" and 200", for initial primary and secondary wire diameter of .5 inch. Later, secondary wire diameters of 0.75 inch and 1.00 inch were also evaluated. For a fixed width of core of 15 inch, core thicknesses of 25, 15, and 5 inches were evaluated. The wire operating temperature was assumed fixed at 173 Kelvin, assuming a thermal heat loss temperature differential of approximately 150 Kelvin. All results were calculated using a computer program written in C. Initial evaluations were obtained at 10 KHz without regard for conductor skin effect. After initial evaluations, a final program modification, adding wire skin effect at 10 KHz was made. Individual losses for both primary and secondary were calculated to observe which loss was dominant and to refine the finally selected wire sizes and the balance between core and winding losses.

Analysis of the resulting total losses in the transformer, included both core losses and winding losses as computed by the program leads to the following conclusions:

Because primary current is 60,000 ampere, the initial results were dominated by primary wire loss. Since the major wire losses occur in the primary, the primary conductor was replaced with a fabricated rectangular slab in order to lower its resistance. Larger diameter wire for the secondary was also then selected in order to cut secondary losses. Larger wire size of course increased the required transformer window dimensions and transformer weight, but not very significantly in comparison with the winding loss reduction. Finally, in order to reduce skin effect and guarantee no localized winding hot spots, hollow wire with a duct at the center

of about 0.3" to flow pressurized liquid hydrogen cooling was assumed for the secondary winding. From the result of data using 0.5 inch diameter wire, which as stated above was known to be too small, gave total losses were about 2.5 megawatts. Winding losses were lower when primary wire's diameter set to be 1.0 inch. This reduction in wire losses however increased considerably the total weight of the transformer. Initial comparisons for both primary and secondary windings assumed the same diameter wire for all cases. An eventual crosssectional area of 30 square inches reduced the final primary losses so that total losses of about 0.9 megawatt were obtained for the entire transformer. The total transformer weight of this final design increased moderately to 2,386 Kg. The resulting design now has core losses of 0.8 megawatt which are higher than copper losses. Again, the objective has been to go for minimum mass: significantly lower losses could be achieved at mass expense by cutting the frequency of operation and working at lower maximum flux density. Under the final design assumptions, the transformer is 62 inches long by 40 inches width and 69" thick, including insulting layer. Wire in primary and secondary are of cross section of 10 square inch and 1 inch diameter respectively.

3.6.4 Switching Losses and Final Power-to-Weight Ratio Results

The design of the PASC transformer, using 0.002" Supermendur core material has been carried out with the highest priority objective of minimizing the mass of the system. There is a trade-off between mass of the final system and the core dissipation and solid state switching losses because the mass of the transformer can be reduced as the switching frequency is increased while the losses will directly increase with switching frequency. In addition, the resulting design is a steady state design: the transformer and all components should be able to last indefinitely providing the cooling requirements are met. The losses in the GTO and thyristor switches (5.3 MWe), have been estimated based upon a switching frequency of 10 KHz with square waveform generated input for the inverter and a full wave rectified waveform for the 100 KV a.c. square wave output of the transformer. The losses were calculated based upon data sheet information from the manufacturer (TOSHIBA SG2500GXH21 units) of the solid state components. If it is decided that a higher mass can be allocated to the power conversion equipment, a lower value of losses can be generated. Although detailed comparisons have not been done it appears that if a mass twice as great as that given below could be tolerated for the PASC system, the losses could be cut to about 1/3 of the 6.3 MW design. The final modified design results, including the reduction of 200 pounds by adding the new control and data/acquisition computer system, are as follows:

Total PASC system mass (transformer, switch matrix, computer system, rectifier, switching interface) = 2749 Kg.
Total PASC system losses = 6.3 MWe at 100 MWe, 10 KHz, 100 KV d.c., 1 K amps.
Power-to-weight ratio at 100 MWe conversion level = 36.4 KWe/Kg.
= 16.53 KWe/lb.

4.0 Final Conclusions and Recommendations

In summary we draw the following conclusions at the end of this project:

a. The PASC concept feasibility to perform computer controlled pulse formation has been successfully demonstrated for a wide range of symmetric bi-polar pulse waveforms (sinusoidal, square wave, and ramp sawtooth), over frequency ranges varying from 60 to 600 Hz. The demonstration has been achieved by actual experiment on a prototype system with very heavy and strong reliance on backup validated computer simulations of the design and the experimental cases which have been measured. Computer performance simulations have been achieved using standard industry programs SPICE[3] and EMTP[2] along with parallel custom written software routines.

b. Demonstration of the power extraction and consolidation processes has used 16 dc power supplies to crudely represent 16 electrode pairs of a Faraday connected MHD generator source. Computer simulation studies (not part of this contract), of the internal dynamic interaction expected between the time-dependent gas dynamics of a Faraday configuration MHD duct and the pulsed PASC C/I power extraction process are continuing to determine to what extent the dynamics of the C/I process are limited by the MHD power duct performance.

c. Computer simulation work, which follows very closely the validated simulations already mentioned above, indicates that C/I using the PASC process can be successfully done for diagonally connected MHD generators as well as for Faraday connected generators. However, the use of the PASC connection for two-terminal, diagonally connected generators offers only the following significant advantages over competing line commutated bulk power inverters:

    c.1 the possibility of control of power factor output without reactive compensation,

    c.2 the direct inversion and the ability to operate in program variable pulse mode over wide frequency range,

    c.3 the ability to generate high purity single frequency sinusoidal waveforms without any significant filtering.

d. For multiple section, diagonally connected subsection generators, the PASC system could provide program variable local current control balancing in place of alternative current shuffle circuits.

e. Although PASC C/I feasibility has beeen demonstrated experimentally only for (zero dc content), bipolar pulse waveforms using transformers for the consolidation and pulse superposition synthesis process, simulation work has shown that the use of capacitors along with inductors will permit the PASC technique to generate any desired monopolar pulse waveform. For monopolar waveform synthesis it may be possible to substitute natural commutation thyristor gating for symmetric mode GTOs.

f. For space-based power conversion from 1.7 K vdc to 100 K vdc at the 100 MW electrical level the power-to-weight conversion ratio has been estimated by calculation to be 36.4 KWe/kg for a complete system as defined in section 3.0.

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g.   For arbitrarily shaped bipolar pulse waveforms, symmetric voltage characteristic GTOs must be employed. These GTOs are now commercially available in sizes to meet almost any PASC system requirement but are expensive and vendor delivery lead times are long. This is because commercial and consummer applications do not have the stringent space-based requirements on mass and efficiency.

h.   Closed-loop control of harmonic generation by PASC systems has been demonstrated and examined using computer simulation. Many other control strategies are available and need to be examined in the future for this technology.

i.   For PASC transformer C/I systems the tradeoffs on number of transformers, transformer material and connection configurations, required inductances, losses, and coupling coefficients need significant further study and research, especially relative to a specific design application.

5.0 References

[1]   Rosa, R. J., Magnetohydrodynamic Energy Conversion, McGraw-Hill, 1968.

[2]   Dommel, H. W., "Digital Computer Solution of Electromagnetic Transients in Single and Multiphase Networks," IEEE Transactions on Power Apparatus and Systems, vol. PAS-88, pp 388-399, April 1969.

[3]   Nagel, L. W., and Peterson, D. O., "SPICE, simulation programs with integrated circuits analysis," ERL-M382, Dept. of Electrical Engineering, University of California, Berkeley, 1973.

[4]   B. A. Francis and W. M. Wonham, "The Internal Model Principle of Control Theory", *Automatica*, Vol. 12, pp. 457-465, 1976.

[5]   Gene F. Franklin, J. David Powell, and Abbas Emami-Naeini, *Feedback Control of Dynamic Systems*, Reading, Mass.: Addison-Wesley Publishing Co., 1987.

[6]   Overview of Dr. C. H. Ting's work on The Continuous Fourier Transform, *RTXpress*, Vol. 1, No. 3, p. 7, December, 1989.

Appendix A -- Source Listings

```
\     Control of Static Inverter
\
\                                    Control Tech Corp.
\                                    June, 1990
\
\
\ set up the fences -- H-FENCE is the bottom of code
HEX
4A00 H-FENCE !
49FE R-TOP !
4A00 H !

\ same as C, but data goes into user data area -- not code area
: D,   1 ALLOT THERE 1- C! ;        \ make sure you use D, an even # of times

DECIMAL

\ Variables
VARIABLE SINTable              \ allocation for the 200 byte array SINTable


0 D, 1 D, 2 D, 3 D, 4 D, 5 D, 6 D, 7 D, 8 D, 9 D,
10 D, 11 D, 12 D, 13 D, 14 D, 15 D, 16 D, 17 D, 18 D, 19 D,
20 D, 21 D, 22 D, 23 D, 24 D, 25 D, 26 D, 27 D, 28 D, 29 D,
30 D, 31 D, 32 D, 33 D, 34 D, 35 D, 36 D, 37 D, 38 D, 39 D,
40 D, 41 D, 42 D, 43 D, 44 D, 45 D, 45 D, 46 D, 47 D, 48 D,
49 D, 50 D, 51 D, 52 D, 53 D, 54 D, 55 D, 56 D, 57 D, 57 D,
58 D, 59 D, 60 D, 61 D, 62 D, 63 D, 64 D, 65 D, 65 D, 66 D,
67 D, 68 D, 69 D, 70 D, 71 D, 71 D, 72 D, 73 D, 74 D, 75 D,
76 D, 76 D, 77 D, 78 D, 79 D, 80 D, 80 D, 81 D, 82 D, 83 D,
83 D, 84 D, 85 D, 86 D, 86 D, 87 D, 88 D, 89 D, 89 D, 90 D,
91 D, 92 D, 92 D, 93 D, 94 D, 94 D, 95 D, 96 D, 96 D, 97 D,
98 D, 98 D, 99 D, 100 D, 100 D, 101 D, 101 D, 102 D, 103 D, 103 D,
104 D, 104 D, 105 D, 106 D, 106 D, 107 D, 107 D, 108 D, 108 D, 109 D,
109 D, 110 D, 111 D, 111 D, 112 D, 112 D, 112 D, 113 D, 113 D, 114 D,
114 D, 115 D, 115 D, 116 D, 116 D, 117 D, 117 D, 117 D, 118 D, 118 D,
119 D, 119 D, 119 D, 120 D, 120 D, 120 D, 121 D, 121 D, 121 D, 122 D,
122 D, 122 D, 123 D, 123 D, 123 D, 123 D, 124 D, 124 D, 124 D, 124 D,
125 D, 125 D, 125 D, 125 D, 126 D, 126 D, 126 D, 126 D, 126 D, 126 D,
127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D,
127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D, 127 D,
HEX
4500 R !                        \ CFT Table starts @ 4500H
DECIMAL
VARIABLE CFTTable              \ allocation for the CFT window
998  ALLOT

HEX
\ Set up the user memory location to point to the first free location.
4440 UBR!
DECIMAL
```

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```
\ Variable Initialization
\    these are the 32 allowable user memory location definitions
0 0 U!                                  \ sine table pointer -- Reset to use in SINGEN.
\ Actual freq is (samp. freq)*Ts/T -- in this case (2kHz) * 3 / 100 = 60 Hz.
3 1 U!                                  \ Ts
100 2 U!                                \ T
\ 3-8 are digital filter coefficients
\ 3                                     - b0 numerator
\ 4                                     - b0 denominator
\ 5                                     - b1 num
\ 6                                     - b1 den
\ 7                                     - a1 num
\ 8                                     - a1 den
0 9 U!                                  \ the latest filter output
0 10 U!                                 \ intermediate value for filter calculations
0 11 U!                                 \ intermediate value for filter calculations
100 12 U!                               \ digital filter gain
\ 13                                    - real part of the 3rd harmonic after cft
\ 14                                    - the imag part of above
\ 15                                    - real part of the 12th harmonic after cft
\ 16                                    - the imag part of above
FALSE 19 U!                             \ a flag indicating that cft data is valid
FALSE 20 U!                             \ a flag indicating an overflow in the cft
\ 21                                    - difference between most recent a/d value
\                                       -   and the most distant a/d value for cft
\ 22-30                                 - not used
4500 30 U!                              \ cft table index pointer
\ 31                                    - count delay while waiting for valid cft data

\ CFT constants are arguments for 3rd and 12th harmonics
30 CONSTANT 3RDarg                      \ 800 37 1000 */
116 CONSTANT 12THarg                    \ 800 145 1000 */


: SIN ( n1 -- n2 )
\ n2 is the sin of n1.
\ n2 is between -128 and 128 which represents -1 to 1.
\ SINTable is a table holding 200 points of the first quarter of the sin wave.
    796 MOD                             \ Fold over so it is between 0 and 796.
    DUP 199 < IF
        SINTable + C@  ELSE             \ get SINTable(n+1)
    DUP 398 < IF
        398 SWAP- SINTable + C@ ELSE    \ get SINTable(399-n)
    DUP 597 < IF
        396 - SINTable + C@ NEGATE ELSE \ get -SINTable(n-397)
    DUP 796 < IF
        795 SWAP- SINTable + C@ NEGATE  \ get -SINTable(796-n)
    THEN THEN THEN THEN
    ;
\ end of SIN
```

```
: SINGEN ( -- n )
\ Places the next value of the sin wave on the stack.
\ SINIndex is used to store the position of the sin wave (it is incremented).
\ Ts (samp. per.) and T (sin per.) are used to scale the sin wave.
     0 U@                         \ SINIndex is 0
     2 U@ MOD                     \ wrap the index around -- 2 is T
     DUP 1+ 0 U!
     1 U@ 796 * 2 U@ */           \ n2 * Ts * 796 / T -- 1 is Ts
     SIN
   ;
\ end of SINGEN

HEX

: OUTWORD ( n1 -- )
\ Staircase limit n1, and send the switch word to the appropriate
\ ASIC bus address.
DUP -FF > IF
   FFFF 1A G!
   DUP EF1 > IF
      0000 ELSE                   \ level 8
   DUP CF3 > IF
      0080 ELSE                   \ level 7
   DUP AF5 > IF
      0060 ELSE                   \ level 6
   DUP 8F7 > IF
      001C ELSE                   \ level 5
   DUP 6F9 > IF
      00C3 ELSE                   \ level 4
   DUP 4FB > IF
      003E ELSE                   \ level 3
   DUP 2FD > IF
      00F9 ELSE                   \ level 2
   DUP FF > IF
      00F7 ELSE                   \ level 1
      00FF                        \ level 0
   THEN THEN THEN THEN THEN THEN THEN THEN
   SWAP DROP
   19 G!                          \ Positive ASIC bus address
THEN
DUP -FF <= IF
   FFFF 19 G!
   DUP -2FD > IF
      00F7 ELSE                   \ level -1
   DUP -4FB > IF
      00F9 ELSE                   \ level -2
   DUP -6F9 > IF
      003E ELSE                   \ level -3
   DUP -8F7 > IF
      00C3 ELSE                   \ level -4
   DUP -AF5 > IF
      001C ELSE                   \ level -5
```

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```
        DUP -CF3 > IF
            0060 ELSE                   \ level -6
        DUP -EF1 > IF
            0080 ELSE                   \ level -7
            0000                        \ level -8
        THEN THEN THEN THEN THEN THEN THEN
        SWAP DROP
        1A G!                           \ Negative ASIC bus address
    THEN
;
\ end of OUTWORD

DECIMAL

: FILTER ( n1 -- n2 )
\ Apply the controller filter C(z) to n1 and return the filtered value
\ on the stack.  n2 is also stored in ylast for future use.
\ The filter coefficients are stored in b0num, b0den, b1num, b1den,
\ a1num, and a1den.  The filter is evaluated in transposed direct form II:
\     y    = intf1 + b0*x
\     intf1 = intf2 + a1*y + b1*x
\     intf2 = a2*y
\ and a2 = -1.
    DUP 3 U@ 4 U@ */            \ b0*x
    10 U@ +                     \     + intf1
    DUP DUP 9 U!                \           = ylast
    ROT 5 U@ 6 U@ */            \ b1*x
    SWAP 7 U@ 8 U@ */ +         \     + a1*y
    11 U@ +  10 U!              \            + intf2 = intf1
    DUP NEGATE 11 U!            \ a2*y = intf2
;
\ end of FILTER

: SETFILTCOEFFS ( -- )
\ Set up the controller filter, C(z), coefficients: b0num, b0den, b1num, b1den,
\ a1num, and a1den.
\ Actual reference frequency is (samp. freq) * Ts / T
\ a1 = -2*cos(w0*Ts)
\ a2 = 1
\ b0 = k2
\ b1 = -k2*cos(w0*Ts)
\ k2 is scaled by 100
12 U@ DUP 3 U! 100 4 U!   ( k2 -- )             \ b0num and b0den
9976 10000 */ 5 U! 1 6 U! ( -- )      \ b1num and b1den
19952 7 U! 10000 8 U!     ( -- )      \ a1num and a1den
;
\ end of SETFILTCOEFFS


HEX
\ Power down and quit if keystroke is caught
: STOPWAVE  ( -- )
    FFFF 001F G!                                \ Send open signals
```

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```
;
\ end of STOPWAVE  ·
DECIMAL

: CLOSEDLOOP  ( -- )
\ Open loop sine wave generator.
    CR@ UBR@                     \ Save the Configuration Reg and UBR
    17472 UBR!                   \ set UBR to 4540H
    SINGEN                       \ Next sine wave point.
    28 G@                        \ Get A/D value and start next conversion.
    255 AND                      \ Look at least significant 8 bits.
    DUP 30 U@ C!                 \ store into cft table - 30 contains table index
    30 U@ 1+ DUP 18663 > IF DROP 17664 THEN    \ check for table wrap
    30 U!                        \ increment the table index  17920 = 4600H
    128 -                        \ Center it at zero.
    -                            \ Find the difference.
    30 *                         \ For numerical scaling.
    FILTER                       \ Apply the controller filter G(z).
    OUTWORD      \ Staircase limit the output, and send it to the ASIC bus.
    TRUE 19 U!                   \ ok to do an fft calc
    UBR! CR!                     \ Restore the Configuration Reg and UBR
    ;
\ end of CLOSEDLOOP


: CFT ( -- )
    BEGIN
\ stop and open gto's on keystroke
    KEY? IF TIMER2 MASK STOPWAVE QUIT THEN
\ ydiff = y ( k ) - y ( k-N ) where N is window length
    30 U@ C@                     \ 30 is addr of most recent y
    128 -                        \ center it -- a/d is 0 -5 volts
    30 U@ 1+ DUP 18663 > IF DROP 17664 THEN \ check for table wrap
    C@                           \ 30 1+ is addr of oldest y
    128 -                        \ center it
    - 21 U!
\ get last step index
    14 U@ DUP 1+ 500 MOD 14 U!                        ( step -- )
\ 3arg corresponds to -2*pi*i*k*n/N , the argument of the CFT exponential
    DUP 3RDarg 796 */MOD DROP                ( step 3arg -- )
    DUP SIN                                   ( step 3arg sin -- )
\ the imaginary part of the exponential
    21 U@ * 16 U@ + DUP 16 U!                 ( step 3arg imag -- )
    DUP ABS 180 > IF TRUE 20 U! THEN         \ check for overflow
    DUP *                                     ( step 3arg imag^2 -- )
    SWAP 199 + 796 MOD SIN       ( step imag^2 cos -- )
\ the real part of the exponential
    21 U@ * 15 U@ + DUP 15 U!                 ( step imag^2 real -- )
    DUP ABS 180 > IF TRUE 20 U! THEN         \ check for overflow
    DUP *                                     ( step imag^2 real^2 -- )
\ the magnitude of the exponential
    + SQRT 100 *                              ( step |3rd| -- )
```

```
\ start on 12th harmonic
\ 12arg is same as 3arg but for 12 harmonic
      SWAP 12THarg 796 */MOD DROP            ( |3rd| 12arg -- )
      DUP SIN                                ( |3rd| 12arg sin -- ) ,
\ the imaginary part of the exponential
      21 U@ * 18 U@ + DUP 18 U!              ( |3rd| 12arg imag -- )
      DUP ABS 180 > IF TRUE 20 U! THEN       \ check for overflow
      DUP *                                  ( |3rd| 12arg imag^2 -- )
      SWAP 199 + 796 MOD SIN      ( |3rd| imag^2 cos -- )
\ the real part of the exponential
      21 U@ * 17 U@ + DUP 17 U!              ( |3rd| imag^2 real -- )
      DUP ABS 180 > IF TRUE 20 U! THEN       \ check for overflow
      DUP *                                  ( |3rd| imag^2 real^2 -- )
\ the magnitude of the exponential
      + SQRT                                 ( |3rd| |12th| -- )
\ take ratio and adjust controller gain
      / DUP                                  ( ratio ratio -- )
\ this is a delay to wait for valid data -- also dont do another point
\      until an interrupt has occured -- 19 is set true in interrupt
      31 U@ DUP 32000 < IF 1+ 31 U! FALSE 19 U! ELSE DROP THEN
\ a true flag means data valid
      19 U@                                  ( ratio ratio flag -- )
      DUP ROT                                ( ratio flag ratio flag -- )
      AND 110 > IF 12 U@ 1+ 12 U! SETFILTCOEFFS THEN   ( ratio flag -- )
      90 AND < IF 12 U@ 1- 12 U! SETFILTCOEFFS THEN   ( -- )
\ if there was an overflow, start over with new data
      20 U@ UNTIL FALSE 20 U!
    ;

: STARTCLOSED ( -- )
\ Start the open loop driver by enabling the timer 0 interrupt which runs
\ CLOSEDLOOP at each interrupt.
    SETFILTCOEFFS
    4000 TC2!
    ['] CLOSEDLOOP 9 !INTERRUPT
    TIMER2 UNMASK
    BEGIN
      0 31 U!                      \ a flag to indicate valid data in the cft table
      CFT
    AGAIN
    ;
\ end of STARTCLOSED
```